MEMORIES
MICRO-PROCESSORS
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MOSTEK

MOS INTEGRATED CIRCUIT GUIDE

Numerical/Functional Index

MEMORIES

Mostek offers a broad line of memory products – all with state-of-the-art technology and specifications. In this section you'll find a complete family of 4K dynamic RAMs (in the industry standard 16-pin package) plus a selection of 1K statics and dynamics, Read Only Memories and shift registers.

MICRO-PROCESSORS

The F-8 microprocessor from Mostek is a complete family of MOS circuits that can be used as building blocks to construct versatile, efficient, cost effective systems from simple to complex. Design versatility is achieved with a minimum 2-chip system, expandable to 5 or more. Cost effectiveness, another big advantage to the F-8, is achieved through minimum parts count in the system. Evaluation is simplified with the F-8 Evaluation Kit.

CONSUMER CIRCUITS

Mostek offers unique consumer circuits for a variety of applications - calculators, radio alarm clocks, watches and clocks. All in high volume production, with features to help your product sell.

INDUSTRIAL

With the growing need for solid-state reliability and cost efficiency in industrial application, Mostek offers a growing selection of timers, counter/decoders and frequency generators.

FUTURE PRODUCTS

At Mostek there's a continuing development of new products...and improvements in existing products. In this section we highlight several "soon-to-be-announced" designs. For a complete update on the latest developments in MOS – call Mostek.

MEMORIES

MICRO-
PROCESSORS
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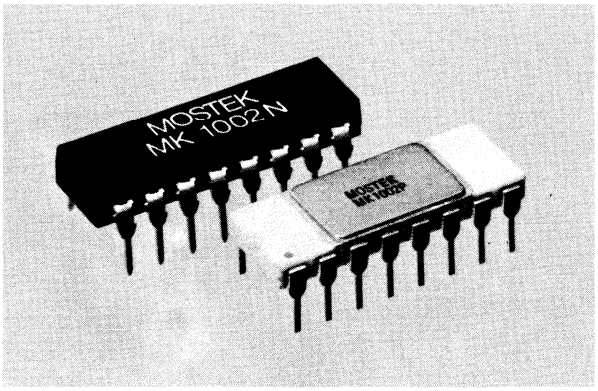
CIRCUITS
INDUSTRIAL
FUTURE
PRODUCTS

MOSTEK

MK 1002 P
MK 1002 N

DUAL 128-BIT
MOS Static Shift Register

MOSTEK



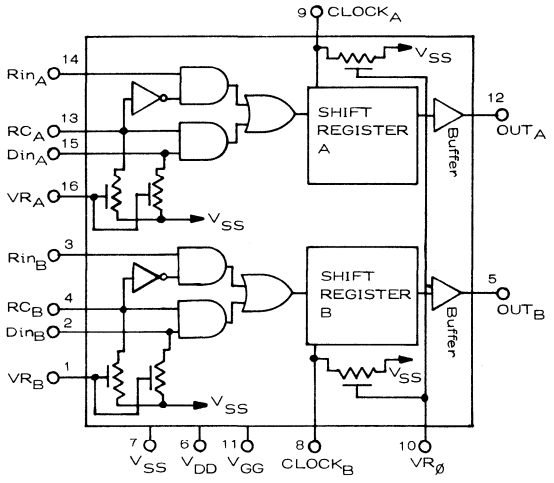
FEATURES:

- ☐ Ion-implanted for full TTL/DTL compatibility — no interface circuitry required
- ☐ Single-phase, TTL/DTL compatible clocks
- ☐ Dual 128-bit static shift registers — 256 bits total
- ☐ Dual sections have independent clocks
- ☐ Recirculate logic built in
- ☐ DC to 1 MHz clock rates
- ☐ Low power dissipation — 130 mW
- ☐ 16-pin dual-in-line package

APPLICATIONS

- ☐ Delay lines
- ☐ Buffer data storage
- ☐ Recycling test data sequencer
- ☐ Digital filtering

FUNCTIONAL DIAGRAM



DESCRIPTION

The MK 1002 is a P-channel MOS static shift register utilizing low threshold-voltage processing and ion-implantation to achieve full TTL/DTL compatibility. Each of the two independent 128 bit sections has a built-in clock generator to generate three internal clock phases from a single-phase TTL-level external input. In addition, each section has input logic for loading or recirculating data within the register. (See Functional Diagram.) The positive-logic Boolean expression for this action is:

OUT (delayed 128 bits) = $(R_C)(D_{in}) + (\overline{R_C})(R_{in})$

The Data, Recirculate Control, and Clock inputs are provided with internal pull-up resistors to V_{SS} (+5V) for use when driving from TTL. These resistors can be disabled when driving from circuitry with larger output-voltage swings, such as DTL. Enabling of pull-up resistors is accomplished by connecting the appropriate terminal to V_{GG}; disabling by connecting to V_{SS}. The Recirculate inputs are not provided with pull-up resistors since they are generally driven from MOS.

Shifting data into the register is accomplished while the Clock input is low. Output data appears following the positive-going Clock edge. Data in each register can be held indefinitely by maintaining the Clock input high.

OPERATING NOTES

R_C	R_{in}	D_{in}	DATA ENTERED
1	X	1	1
1	X	0	0
0	1	X	1
0	0	X	0

"1" = V_{SS} = +5V
"0" = V_{DD} = Grd
X = No Effect
Output Logic: See Description.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} . . . . . V_{SS} — 10.0 V
Supply Voltage, V_{GG} . . . . . V_{SS} — 20.0 V
Voltage at any Input or Output . . . . . V_{SS} + 0.3 V to V_{SS} — 10.0 V
Operating Free-air Temperature Range . . . . . 0°C to +75°C
Storage Temperature Range . . . . . —55°C to +150°C

RECOMMENDED OPERATING CONDITIONS ($0°C \leq T_A \leq 75°C$)

		PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{SS}	Supply Voltage	4.75	5.0	5.25	V	$V_{DD} = 0$ V
	V_{GG}	Supply Voltage[1]	—12.6	—12.0	—11.4	V	
INPUTS	V_{IL}	Input Voltage, Logic 0[2]		0	V_{SS}—4	V	
	V_{IH}	Input Voltage, Logic 1	V_{SS}—1	5.0	V_{ss}	V	
INPUT TIMING	f	Clock Repetition Rate	DC		1	MHz	
	$t_{\phi p}$	Clock Pulse Width	0.35		10	μs	
	$t_{\phi d}$	Clock Pulse Delay	0.4			μs	See
	$t_{\phi r}$	Clock Pulse Risetime	.010		0.2	μs	Timing
	$t_{\phi f}$	Clock Pulse Falltime	.010		0.2	μs	Diagram
	t_{dld}	Data Leadtime	50			ns	
	t_{dlg}	Data Lagtime	200			ns	
	t_{rld}	Recirculate Control Leadtime	100			ns	
	t_{rlg}	Recirculate Control Lagtime	300			ns	

ELECTRICAL CHARACTERISTICS

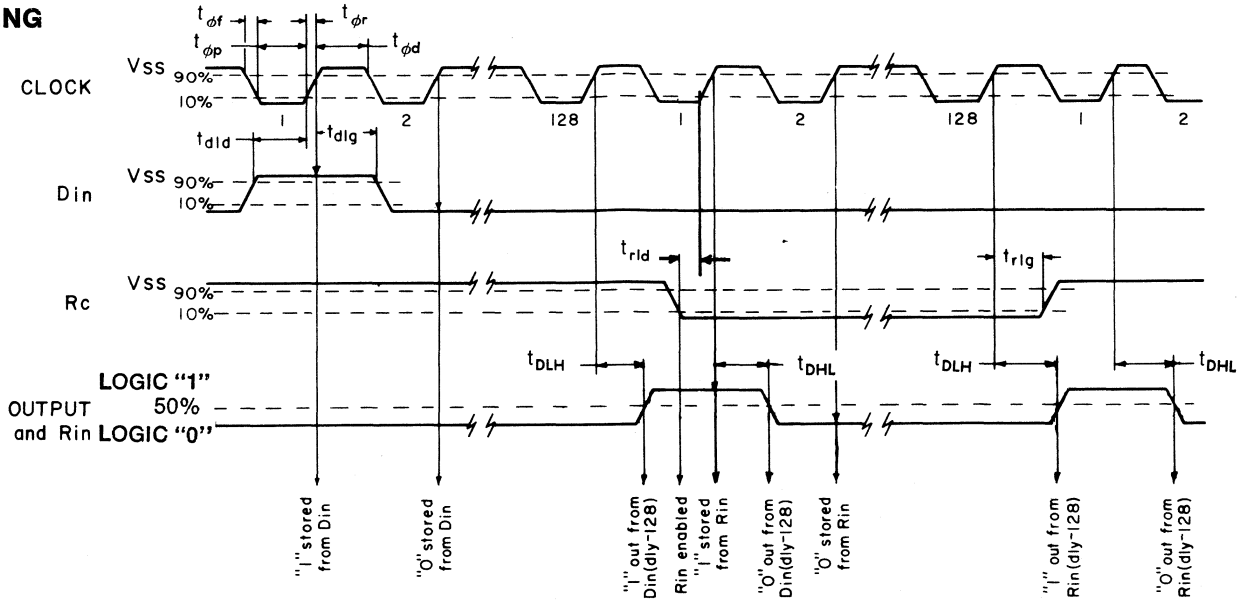
($V_{SS} = +5 \pm 0.25V, V_{GG} = -12 \pm 0.6V, V_{DD} = 0V, T_A = 0°C$ to $+75°C$, using test circuit shown, unless otherwise noted.)

		PARAMETER	MIN	TYP[3]	MAX	UNITS	CONDITIONS
POWER	I_{SS}	Power Supply Current, V_{SS}		14	25	mA	$f_\phi = 1$ MHz Inputs & Outputs open
	I_{GG}	Power Supply Current, V_{GG}		5	10	mA	
INPUTS	C_i	Input Capacitance, any Input		3	10	pF	$V_I = V_{SS}$, f = 1 MHz $T_A = 25°C$
	I_{IL}	Input Current, Logic 0: Resistors Disabled[2]			−40	μA	$V_I = V_{SS} - 5V$
		Resistors Enabled[2]	−0.3		−1.6	mA	$V_I = +0.4V$
	I_{IH}	Input Current, Logic 1, Any Input			40	μA	$VR_A, VR_B, VR\phi = V_{SS}$ $V_I = V_{SS}$
	$I_{IR(on)}$	Input Current at Recirculate Inputs[2]			−40	μA	$VR_A, VR_B, VR\phi = V_{GG}$ $V_I = V_{SS} - 5V$
OUTPUTS	V_{OL}	Output Voltage, Logic 0 (3)			0.4	V	$I_L = -1.6$ mA
	V_{OH}	Output Voltage, Logic 1 (3)	$V_{SS} - 1$			V	$I_L = +100\ \mu A$
DYNAMIC CHAR.	t_{DLH}	Output Delay, Low to High (3)			450	ns	See Timing Diagram and Test Circuit
	t_{DHL}	Output Delay, High to Low (3)			450	ns	
	t_{VOR}	Output Voltage Rise Time (3)		100	150	ns	
	t_{VOF}	Output Voltage Fall Time (3)		100	150	ns	

NOTES:

1. Other supply voltages are permissible providing that supply and input voltages are adjusted to maintain the same potential relative to V_{SS}, e.g., $V_{SS} = 0V$, $V_{DD} = -5 \pm 0.25V$, $V_{GG} = -17 \pm 0.85V$.
2. MOS pull-up resistors to +5V are provided internally. These MOS resistors are enabled by connecting VR_A, VR_B and $VR\phi$ to V_{GG}, and disabled by connecting VR_A, VR_B and $VR\phi$ to V_{SS}. Pull-up resistors not provided at recirculate inputs.
3. At $T_A = 25°C$.

TIMING



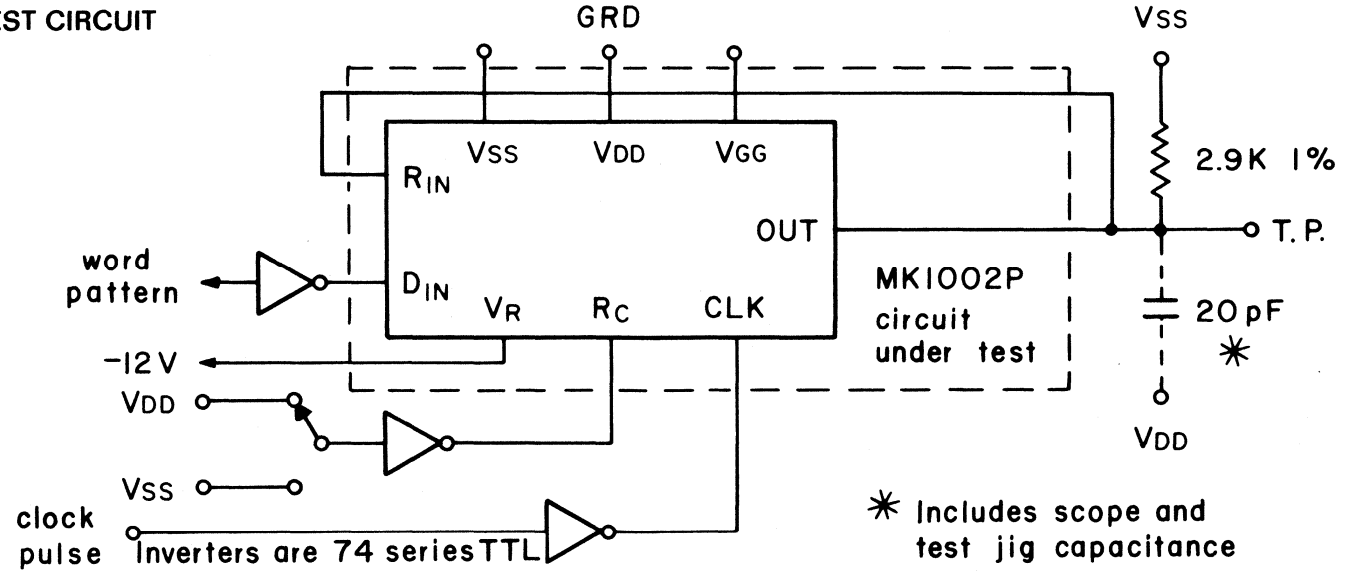
The timing diagram applies to either section of the dual shift register. The test conditions for these waveforms are illustrated below. A logic "1" is defined as +5 V and a logic "0" is defined as 0V

As long as R_C is at a "1", R_{in} is disabled and D_{in} is enabled. The data that is present at D_{in} while the clock is at "0" is shifted in and will be stored as the clock goes to a "1" This data must have been present t_{dld} time prior to the clock "1" edge. The data must also remain in that same state for t_{dlg} time after that edge. These times are necessary to insure proper data storage in the first register-cell.

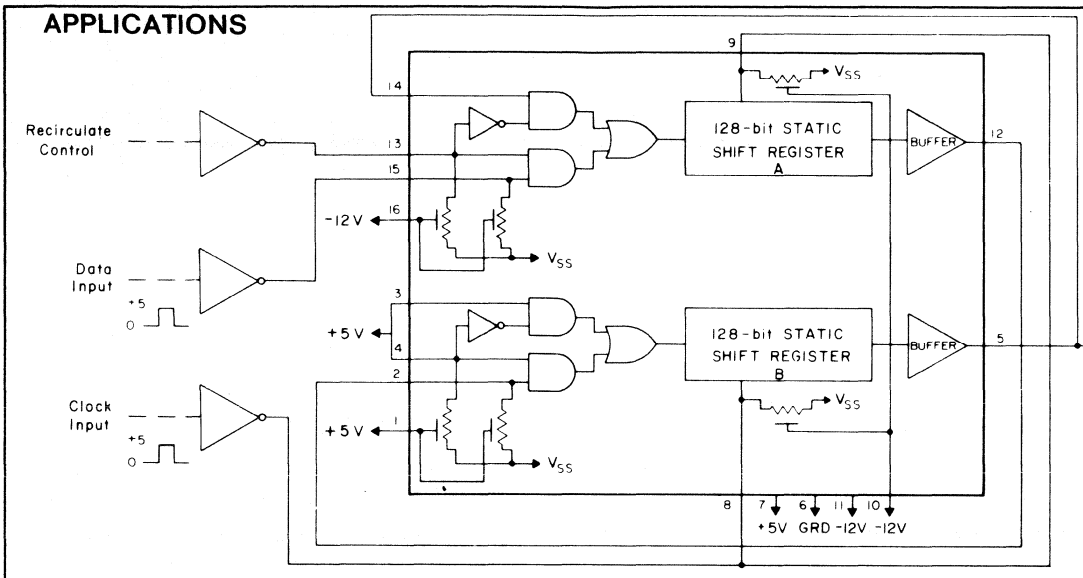
On the clock "1" edge, data is shifted through the register causing bit 127 to be shifted to position 128. This cell's output is buffered and appears at the output in the same logic polarity that appeared at the input 128 clocks prior. This data appears within t_{pd} time of the clock "1" edge.

R_{in} may be hardwired to the data output. When R_C is at a "0", R_{in} is enabled and D_{in} is disabled. Therefore, the output data will appear at the input of the first cell. When R_{in} is tied to the data output, the output delay will insure t_{dlg} and t_{dld} times. R_C "0" time must lead the clock "1" edge by t_{rld} time and must lag that edge by t_{rlg} time to insure proper data storage when recirculate storage is desired.

TEST CIRCUIT



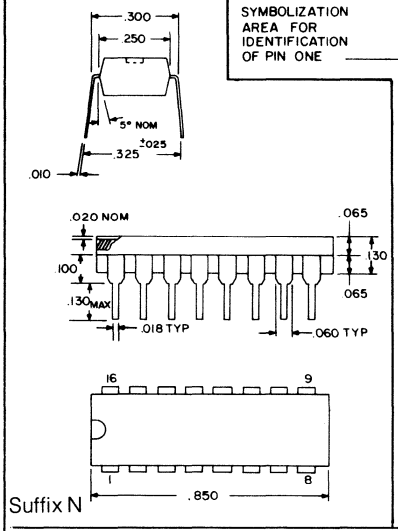
APPLICATIONS



This shows the MK 1002 P connected to operate as a single, 256-bit, static shift register. Pull-up resistors are enabled at TTL driven inputs and disabled at MOS or DTL driven inputs. Any similar TTL/DTL device may be used in place of the inverters shown.

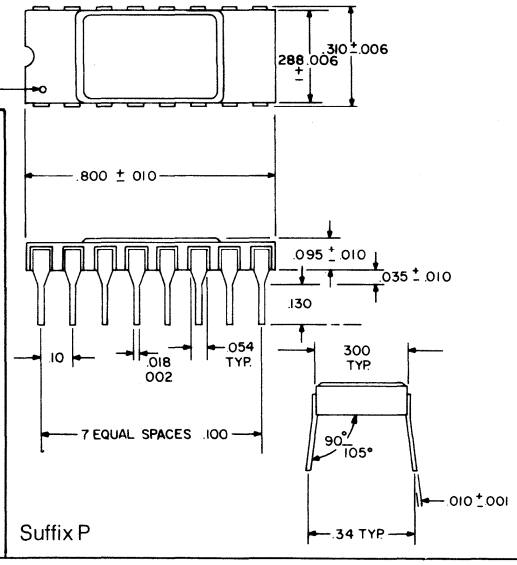
Inverters are 74-series TTL

PACKAGE 16-pin plastic dual-in-line



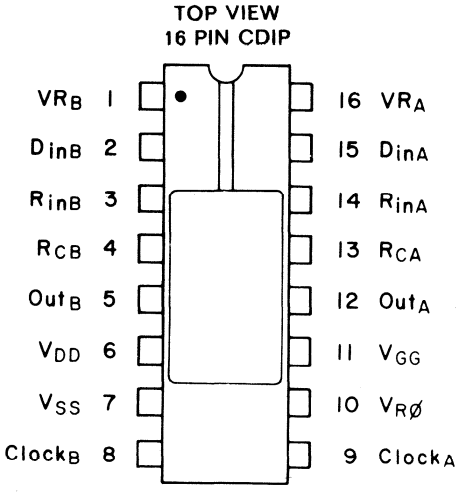
Suffix N

PACKAGE 16-pin ceramic dual-in-line

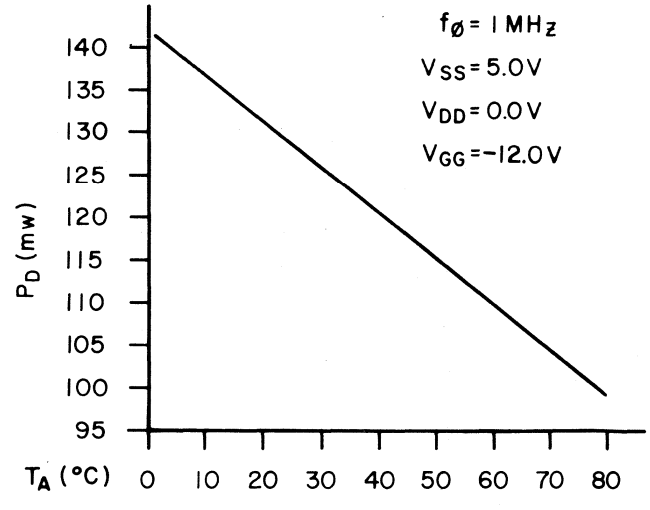


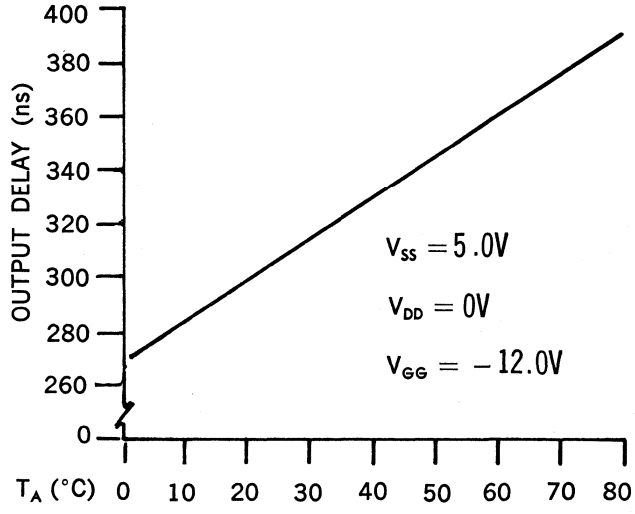
Suffix P

PIN CONNECTIONS



TYPICAL PERFORMANCE

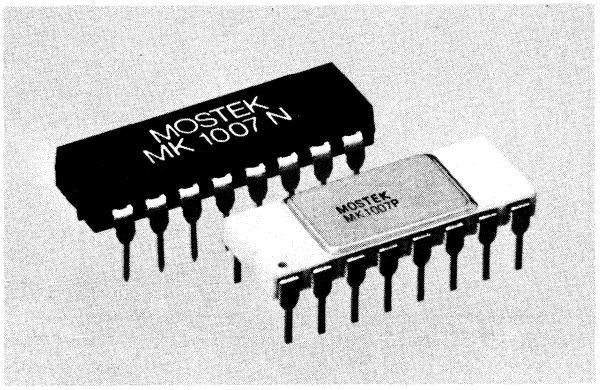




MK 1007P
MK 1007N

MOSTEK

320 Bits (4x80)
MOS Dynamic Shift Register



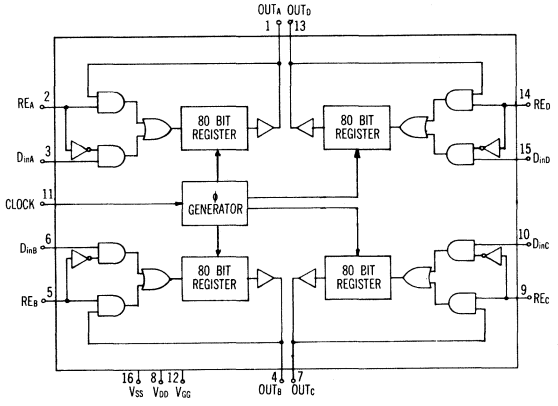
FEATURES:

- ☐ Ion-implanted for full TTL/DTL compatibility
- ☐ Single-phase, TTL/DTL-compatible clock
- ☐ Internal pull-up resistors
- ☐ Clock frequency 10 kHz to 2.5 MHz
- ☐ Built-in recirculate logic for each register
- ☐ Power Supplies: +5V and −12V

APPLICATIONS:

- ☐ CRT display systems
- ☐ Buffer data storage
- ☐ Delay lines
- ☐ Digital filtering

FUNCTIONAL DIAGRAM



DESCRIPTION

The MK 1007 P contains four separate 80-bit MOS dynamic shift registers on a single chip, using ion-implantation in conjunction with P-channel processing to achieve low threshold voltage and direct TTL/DTL compatibility. All logic inputs, including the single-phase Clock, can be driven directly from DTL or TTL logic. Pull-up resistors to +5V are provided for worst-case TTL inputs.

Each 80-bit register has independent inputs and outputs and a control input (RE) which allows external data to be shifted into the register (at logical 0) or data at the output to be recirculated into the register (at logical 1).

All four registers use a common (external) Clock input. With the Clock high (1), data is shifted into the registers. Following the negative-going edge of the Clock, data shifting is inhibited and output data appears. Output data is True, delayed 80 bits.

Since the MK 1007 P has zero lag-time requirements for data inputs, devices may be cascaded, i.e., the output of one device may be fed directly to the input of another device. All inputs are protected to prevent damage due to static charge accumulation.

OPERATING NOTES:

1. Recirculate Enable (RE) = Logic 1 = output data recirculated.
2. Output data (delayed 80 bits) maintains same logic state when RE = 1.
3. Recirculate Enable (RE) = Logic 0 = Data In (D_{in}) enabled.
4. Output data (delayed 80 bits) attains same logic state as D_{in} when RE = 0.
5. Output data follows the clock negative edge.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{DD}	V_{SS} + 0.3 V to V_{SS} − 20 V
Supply Voltage V_{GG}	V_{SS} + 0.3 V to V_{SS} − 20 V
Voltage at any Input or Output	V_{SS} + 0.3 V to V_{SS} − 20 V
Operating Free-air Temperature Range	0°C to 75°C
Storage Temperature Range	−55°C to +150°C

RECOMMENDED OPERATING CONDITIONS

($0°C \leq T_A \leq 75°C$)

	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{SS} Supply Voltage	4.75	5.0	5.25	V	V_{DD} = 0 V
	V_{GG} Supply Voltage[1]	−12.6	−12.0	−11.4	V	
INPUTS	V_{IL} Logic "0" Voltage, any input		0.0	0.8	V	
	V_{IH} Logic "1" Voltage, any input [2]	V_{SS} − 1.5	+5.0	V_{SS}	V	
INPUT TIMING	$f\phi$ Clock Repetition Rate	.01		2.5	MHz	
	$t\phi_p$ Clock Pulse Width	.150		100	μs	NOTE: Total permitted clock times will be determined by clock frequency, $f\phi$.
	$t\phi_d$ Clock Pulse Delay	.150		100	μs	
	$t\phi_r$ Clock Pulse Risetime	.010		5	μs	
	$t\phi_f$ Clock Pulse Falltime	.010		5	μs	
	t_{dld} Data Leadtime	150			ns	
	t_{dlg} Data Lagtime	0			ns	
	t_{rld} Recirculate Control Leadtime	200			ns	
	t_{rlg} Recirculate Control Lagtime	50			ns	

ELECTRICAL CHARACTERISTICS

(V_{SS} = +5 ±0.25 V, V_{GG} = −12 ±0.6V, V_{DD} = 0V, T_A = 0°C to +75°C, unless otherwise specified.)

	PARAMETER	MIN	TYP[3]	MAX	UNITS	CONDITIONS
POWER	I_{SS} V_{SS} Power Supply Current[4][5]		22.0	40.0	mA	$f\phi$ = 2.5 MHz;
	I_{GG} V_{GG} Power Supply Current[5]		9.0	16.0	mA	outputs open
INPUTS	C_{IN} Capacitance at Data, RE, and Clock Inputs[5]		3	6	pF	$V_I = V_{SS}$, $f\phi$ = 1 MHz
	I_{IL} Logic "0" Current, any input[5]	0.6	1.1	1.6	mA	V_I=0.4 V
	$I_{I(lk)}$ Leakage Current, any input			1	μA	$V_I=V_{SS}-5.5V$; $V_{SS}=V_{DD}=V_{GG}$
	R_{IN} Input Pullup Resistance[5]	3.0		8.4	kΩ	V_I=0.4 V
OUTPUTS	V_{OL} Logic "0" Output Voltage[5]			0.4	V	I_L = −1.6 mA
	V_{OH} Logic "1" Output Voltage[5]	V_{SS} − 1			V	I_L = +100 μA
DYN. CHAR.	t_{DLH} Output Delay, Low to High		75	200	ns	See Timing Diagrams
	t_{DHL} Output Delay, High to Low		75	200	ns	
POWER DIS.	$P_{D(1)}$ Power Dissipation[4]		220		mW	$f\phi$ = 2.5 MHz
	$P_{D(2)}$ Power Dissipation[4]		195		mW	$f\phi$ = 1 MHz
	$P_{D(3)}$ Power Dissipation[4]		170		mW	$f\phi$ = 10 kHz

NOTES:

(1) Other supply voltages are permissible providing that supply and input voltages are adjusted to maintain the same potential relative to V_{SS}, e.g., V_{SS}=0 V, V_{DD}= −5V, V_{GG}= −17 V.
(2) Pull-up resistances to +5V are provided internally.
(3) Typical values at T_A=25°C, V_{SS}=+5.0 V, V_{DD}=−12.0 V.
(4) I_{SS} will increase a maximum of 1.6 mA for each input at logic "0."
(5) At T_A=25°C.

TIMING

CONDITIONS:

1. All timing relationships apply to any of the four registers.
2. Logic 0 is defined as V_{DD} or ground; logic 1 as V_{SS} or +5V.

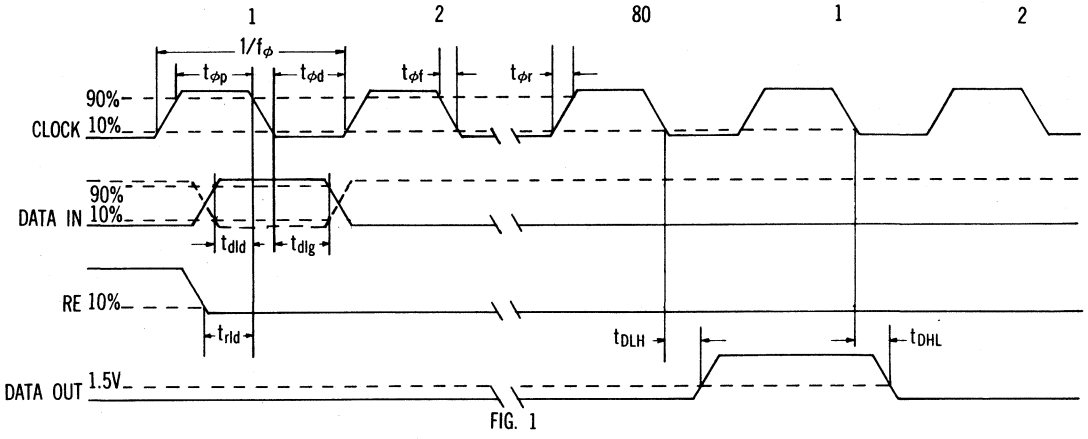


FIG. 1

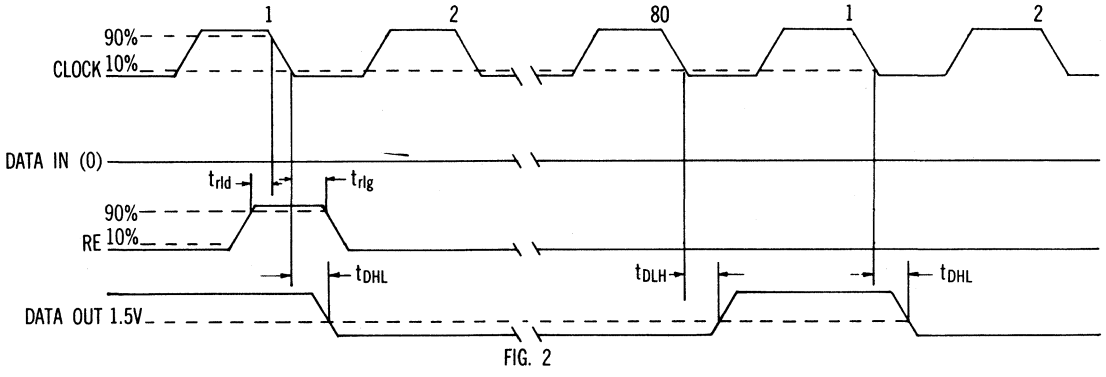
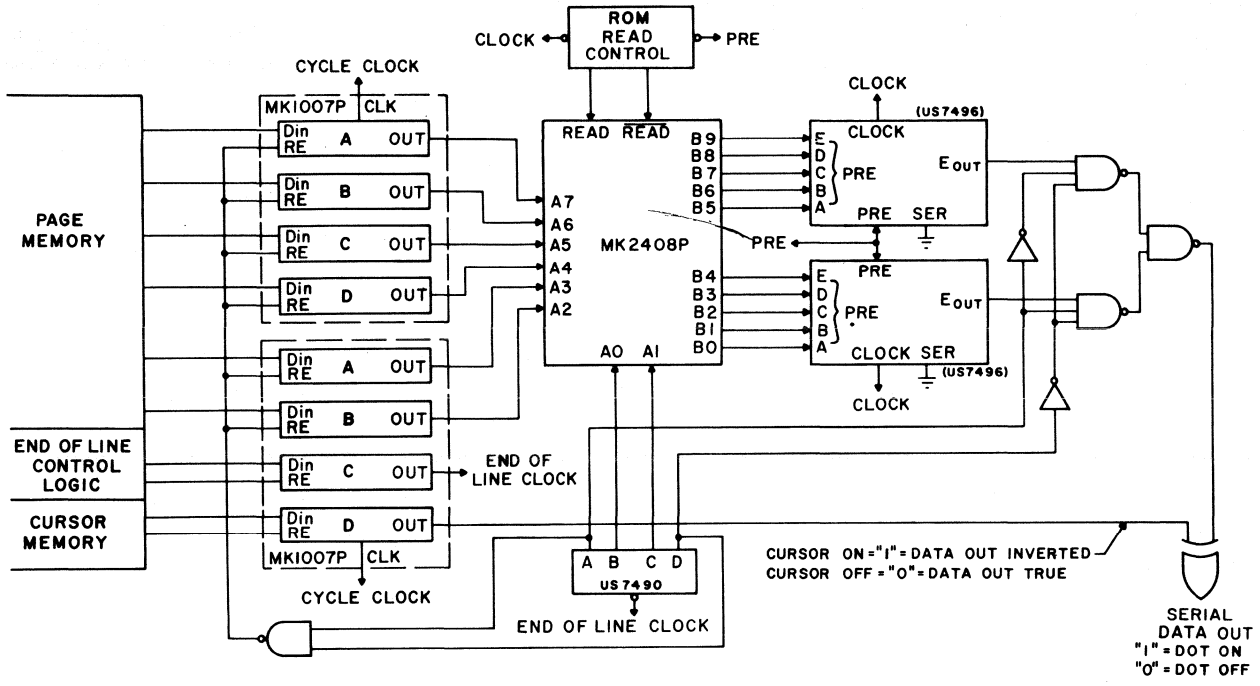


FIG. 2

SHIFT: Fig. 1 illustrates shifting a logic 1 bit from the Data Input (D_{in}) through one of the 80-bit registers. RE (Recirculate Enable) at logic 0 enables D_{in}. RE must go to logic 0 for t_{rld} time (Recirculate Control Leadtime) prior to the Clock's negative edge, and must maintain that state at least until the Clock's negative edge (t_{dlg}) to insure proper data shifting. This data bit entered will appear 80 clock pulses later within Output Delay Time (t_D) of that Clock's negative edge.

RECIRCULATE: Fig. 2 illustrates recirculating a bit present at the output back through the register. RE must attain a logic 1 for t_{rld} time (Recirculate Control Leadtime) prior to the Clock's negative edge, and must maintain that state at least until the Clock's negative edge (t_{rlg}) to insure proper data recirculation. The bit entered will appear 80 clocks later as shown.

APPLICATIONS



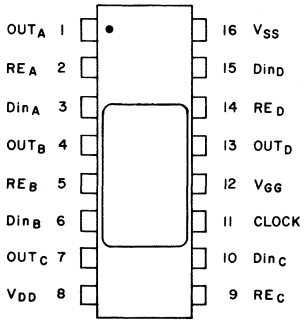
LINE REFRESH MEMORY FOR CRT DISPLAY

This application shows the MK 1007 P used as the Line Refresh Memory, driving MOSTEK's MK 2408 P TTL-compatible character generator. The MK 1007 P receives new data from the Page Memory (which may also consist of MK 1007 P's) on the tenth row of any character line, this being the third vertical space between rows of characters. The MK 1007 P recirculates the character-address data as these characters are scanned and displayed on a CRT screen.

The decade counter selects the appropriate rows from the character generator which outputs two rows of the addressed character at one time (see MK 2408 P data sheet), and also controls the multiplexed output of the character generator so that only one row of the addressed characters is displayed on any CRT horizontal sweep.

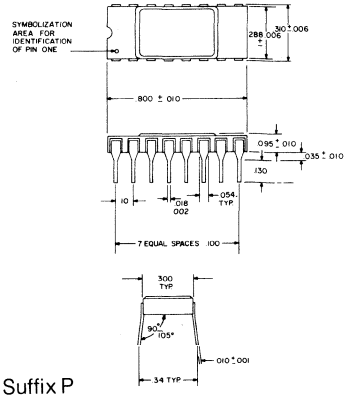
One stage of the MK 1007 P may be used to shift a single data bit, which may be used to determine the end of the horizontal sweep. Another stage may be used as a cursor control and, as shown above, may blank the cursored character dots while surrounding dots are on, to give a reverse image of that particular character.

TOP VIEW
16 PIN CDIP



PACKAGE

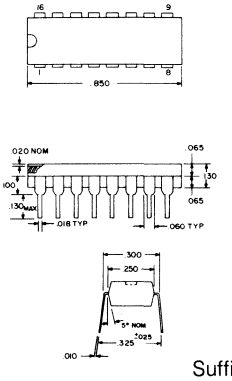
16-pin ceramic dual-in-line



Suffix P

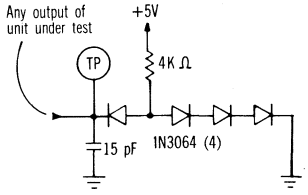
PACKAGE

16-pin plastic dual-in-line



Suffix N

TEST CIRCUIT



2560 BITS (256x10)

MOS Read Only Memory

MOSTEK

FEATURES

- ☐ Ion-implanted for full TTL/DTL compatibility
- ☐ Chip enable permits wire-ORing
- ☐ Custom-programmed memory requires single mask modification
- ☐ 550 ns cycle time ($0° \leq T_A \leq 75°C$)
- ☐ Static output storage latches
- ☐ Optional 3-bit, chip-select decoder available
- ☐ 2560 bits of storage, organized as 256 10-bit words
- ☐ Operates from +5V and −12V supplies

APPLICATIONS

- ☐ Look-up table
- ☐ Code converter
- ☐ Stroke character generator
- ☐ Dot-matrix character generator

DESCRIPTION

The MK 2400 P Series TTL/DTL-compatible MOS Read-Only Memories (ROM's) are designed for a wide range of general-purpose memory applications where large quantity bit storage is required. Each ROM provides 2560 bits of programmable storage, organized as 256 words of 10 bits each. Low threshold-voltage processing, utilizing ion implantation with P-channel enhancement-mode MOS technology, provides direct input/output interface with TTL and DTL logic.

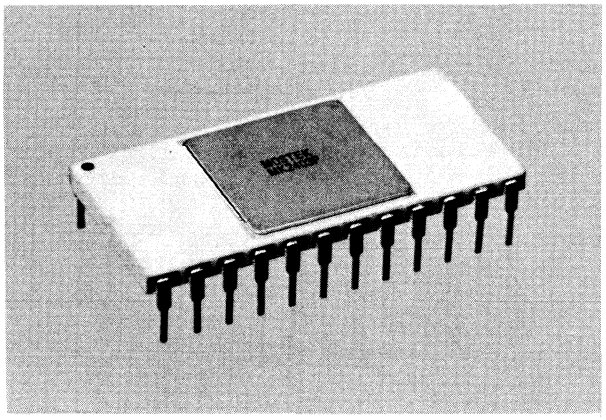
Programming is accomplished during manufacture by modification of a single mask, according to customer specifications. The MK 2400 P Series is available in either 24-lead or 28-lead ceramic dual-in-line packages. On the 28-pin ROM, an optional Chip Select Decoder may also be programmed according to customer specifications to provide a 3-bit Chip Select Code.

Operation involves transferring addressed information from the memory matrix into the storage latches using the READ and $\overline{\text{READ}}$ inputs (see Timing). Information stored in the latches will remain despite address changes or chip disabling until the READ and $\overline{\text{READ}}$ inputs are again cycled. READ and $\overline{\text{READ}}$ input signals may be generated from separate timing circuits if desired, or either may be the inverse of the other.

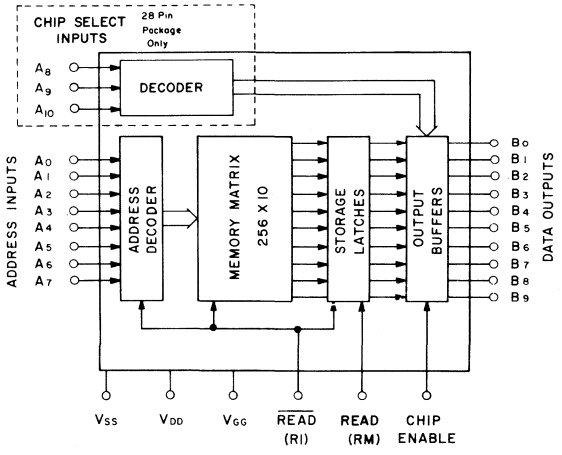
The Chip Enable input forces the normally push-pull output buffer stages to an open-circuit condition when disabling the chip. If desired, new data can be stored in the storage latches while the chip is disabled. When the chip is re-enabled, this data would be present at the outputs.

All inputs are protected against static charge accumulation. Pull-up resistors on all inputs are available as a programmable option.

For additional information regarding custom programming and coding sheets, contact your nearest Mostek representative.



FUNCTIONAL DIAGRAM



OPERATING NOTES

CHIP ENABLE	READ	$\overline{\text{READ}}$	OUTPUT
0	X	X	A
1	0	1	B
1	1	0	C

"1" = V_{SS} (+5V); "0" = V_{DD} (0V)

X = No effect on output

A = Output open-circuited

B = Output retains data last stored in latches

C = Output assumes state of addressed cells

ABSOLUTE MAXIMUM RATINGS

Voltage on any terminal relative to V_{SS} ..... +0.3V to −10V
Operating temperature range ..... 0°C to +75°C
Storage temperature range ..... −55°C to +150°C

RECOMMENDED OPERATING CONDITIONS ($0°C \leq T_A \leq 75°C$)

	PARAMETER		MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{SS}	Supply voltage	+4.75	+5.0	+5.25	V	
	V_{DD}	Supply voltage	—	0.0	—	V	See note 1
	V_{GG}	Supply voltage	−12.6	−12.0	−11.4	V	
INPUTS	$V_{in(0)}$	Input voltage, logic "0"		0	+0.8	V	Pull-up resistors (≈5K~) to
	$V_{in(1)}$	Input voltage, logic "1"	$V_{SS}-1.5$	V_{SS}		V	V_{SS} available as programmable option.
INPUT TIMING	t_{cyc}	Address change cycle time	550			ns	See Timing Section
	t_{ld}	Address to $\overline{\text{Read}}$ lead time	250			ns	
	t_{lg1}	Read lag time 1	−.05		.05	μs	
	t_{lg2}	Read lag time 2	−.05		.05	μs	
	$t_{\overline{rd}}$	$\overline{\text{Read}}$ pulse width	300			ns	
	t_{rd}	Read pulse width	0.3		100	μs	
	t_r	Rise time, any input			100	ns	
	t_f	Fall time, any input			100	ns	

ELECTRICAL CHARACTERISTICS ($V_{SS}= +5.0V \pm 0.25V$, $V_{GG}= -12.0V \pm 0.6V$, $0°C \leq T_A \leq +75°C$, unless noted otherwise. Pull-up resistors not programmed.)

	PARAMETER		MIN	TYP*	MAX	UNITS	CONDITIONS
POWER	I_{SS}	Supply current (V_{SS})		12	25	mA	Outputs unconnected
	I_{GG}	Supply current (V_{GG})		−12	−25	mA	See Note 2 and Note 3
INPUTS	C_{in}	Input capacitance		5	10	pF	$V_{in}=V_{SS}$, $f_{meas}=$ 1MHz
	I_{in}	Input leakage current			10	μA	$V_{in}=V_{SS}-6V$ $T_A=25°C$
OUTPUTS	$V_{out(0)}$	Output voltage, logical "0"			0.4	V	$I_{out}=1.6$ mA (into output)
	$V_{out(1)}$	Output voltage, logical "1"	2.4			V	$I_{out}=0.4$ mA (out of output)
							$V_{SS}-6V \leq V_{out} \leq V_{SS}$
	I_{out}	Output leakage current	−10		+10	μA	$T_A=25°C$ (outputs disabled)
DYNAMIC CHARACTERISTICS	t_{ACC}	Address-to-output access time			600	ns	$t_{ld}=250$ns, $t_{lg1}=0$, $t_{lg2}=0$, See note 4 — See timing Section and Figure #1
	t_{OD}	Output delay time			350	ns	
	t_{OEO}	Output enable/disable time		125	300	ns	
	t_{CS}	Chip Select to Output Delay			600	ns	
	t_{CD}	Chip Deselect to Output Delay			600	ns	

*Typical values apply at $V_{SS}= +5.0V$, $V_{GG}= -12.0V$, $T_A=25°C$

NOTES: 1. Supply voltages shown are for operation in a TTL/DTL system. Other supply voltages may be used if V_{DD} and V_{GG} maintain the same relationship to V_{SS}, e.g., $V_{SS}=0V$, $V_{DD}= -5V$, $V_{GG}=-17V$. Input voltages would also need to be adjusted accordingly.

2. Max measurements at 0°C. (MOS supply currents increase as temperature decreases.) I_{SS} will increase 1.6mA (max) for each input at logic 0 when pull-up resistors are programmed.

3. Unit operated at minimum specified cycle time.

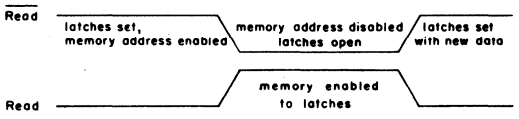
4. The outputs become open circuited when disabled or deselected. As shown in Fig. 1, an output with a "1" expected out does not transition through the 1.5V point when enabled (selected) or disabled (deselected); this is true because the TTL equivalent load pulls the open-circuited output to approximately 2 volts.

TIMING

Notes:

1. All times are referenced to the 1.5V point relative to V_{DD} (ground) except rise and fall time measurements.
2. Chip enable = V_{SS} for all measurements except when measuring T_{OEO}.
3. Logic 0 is defined as V_{DD} or ground; logic 1 as V_{SS} or +5V.

INTERNAL FUNCTION OF READ/$\overline{\text{READ}}$ SIGNALS

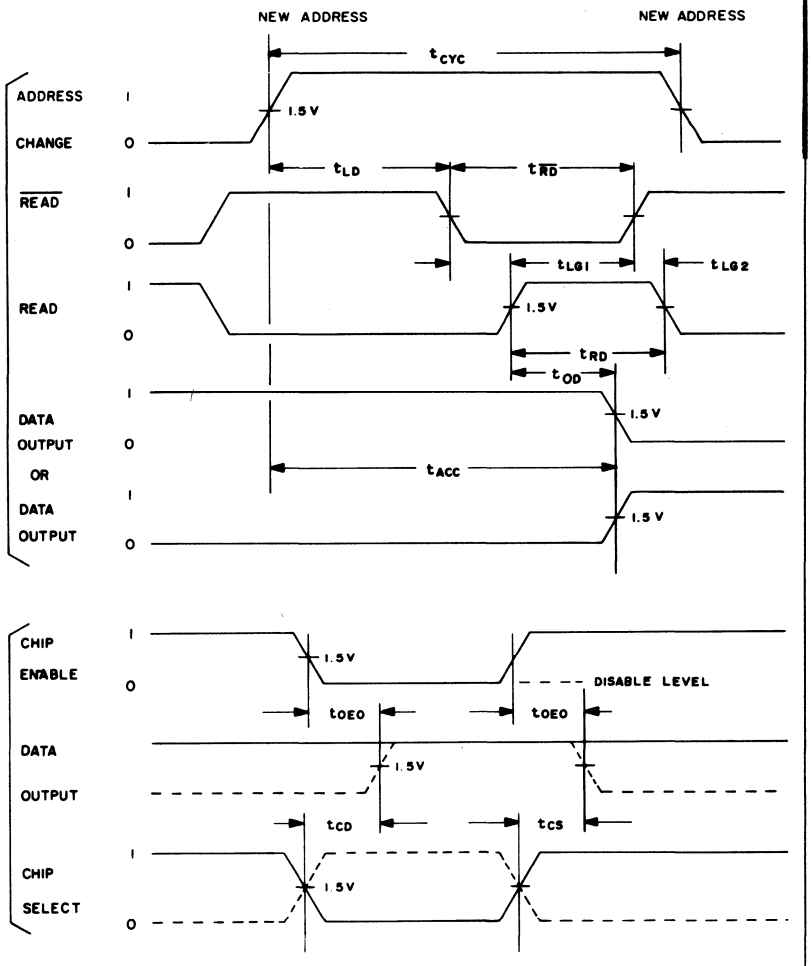


Set up time, t_{Id}, allows the input address to propagate through the address decoder and memory matrix prior to $\overline{\text{READ}}$ logic 0 time. As indicated above, $\overline{\text{READ}}$ at a logic 0 internally disables the input address so that an external address change may occur without affecting the location previously selected. The latches are also readied to receive new data which is enabled from the matrix when $\overline{\text{READ}}$ is at a logic 1. Data is set in the latches when READ is allowed to rise back to its logic 1 state. In actual use, the READ rising and falling edges can precede the falling and rising edges of $\overline{\text{READ}}$, respectively, as implied by the specification of negative read lag times. This allows a very flexible timing relation between the two pulses, in that either input can be the inversion of the other or both may be generated from separate timing circuits.

Output data appears following the rise of the READ pulse but correct output data will not appear until $\overline{\text{READ}}$ has gone low. For this reason, $\overline{\text{READ}}$ is shown preceding READ even though other relationships are allowed. If READ is made to precede $\overline{\text{READ}}$, delay time, t_{OD}, should be referenced to the fall of $\overline{\text{READ}}$ rather than as shown.

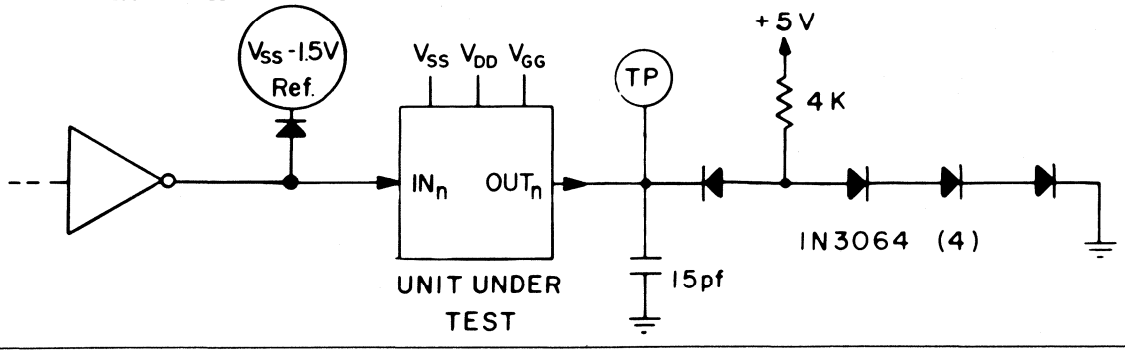
The chip is disabled by applying a logical 0 to the chip enable input, forcing the outputs to an open-circuit condition. The output data present at the time of disable will again be present upon re-enabling unless a new read cycle was initiated for a different address while the chip was disabled, in which case the new data would be present at the outputs.

The programmable 3-bit chip select timing would be the same as the address inputs.

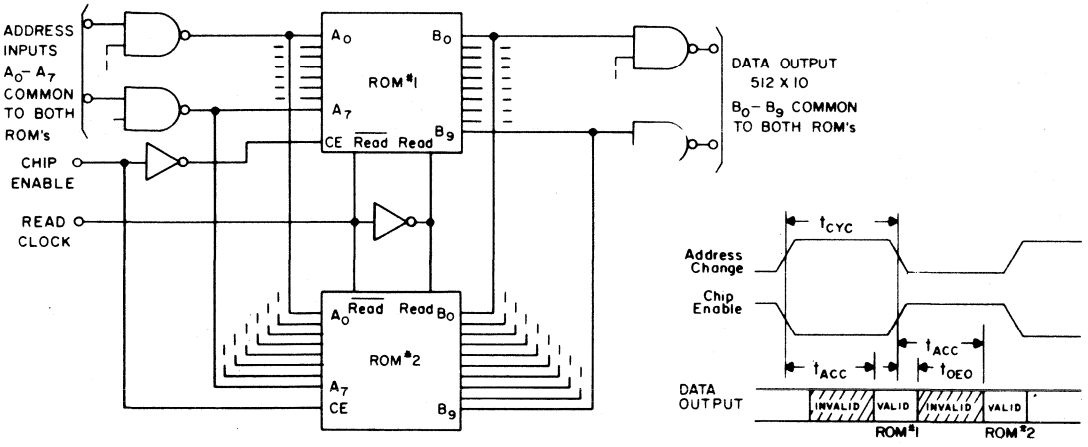


NOTE: Wave forms are not to scale.

FIGURE #1 t_{ACC} and t_{DD} test circuit



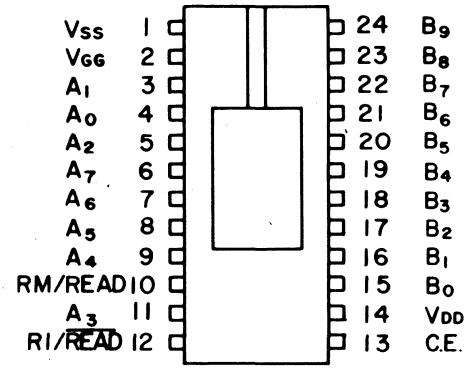
APPLICATIONS



Application shows wire-Or'ing for expansion to a 512 X 10 memory. Further expansion is possible by 1 of N decoding to the Chip Enable input (or with the optional 3-bit decoder) while maintaining the time relationships shown. t_{cyc} should include the desired data-valid time. Interface devices may be TTL or DTL.

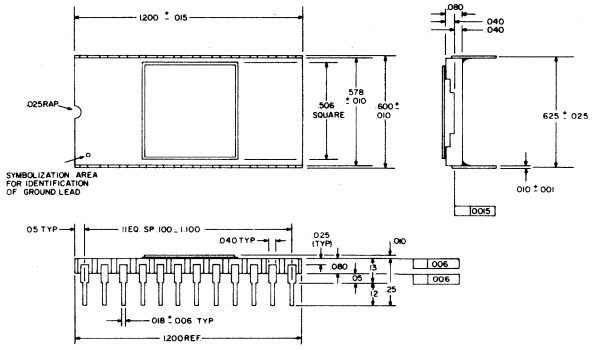
PIN CONNECTIONS

top view, 24 pin CDIP



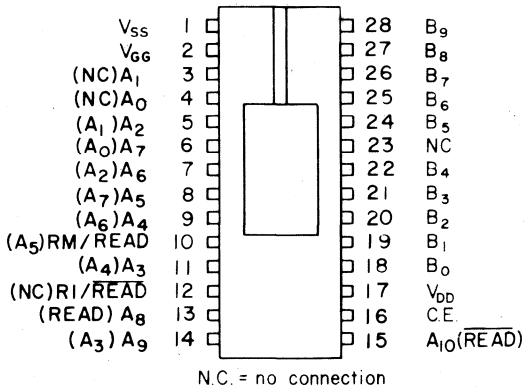
PHYSICAL DESCRIPTION

(24 lead ceramic dual-in-line hermetic package)



PIN CONNECTIONS

top view, 28 pin CDIP

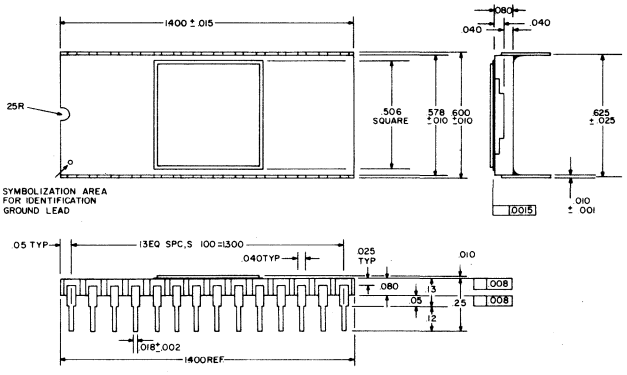


N.C. = no connection

( ) OPTIONAL PIN ARRANGEMENT

PHYSICAL DESCRIPTION

(28 lead ceramic dual-in-line hermetic package)



MOSTEK ROM PUNCHED-CARD CODING FORMAT[1]

MK 2400 P

Cols.	Information Field
First Card	
1-30	Customer
31-50	Customer Part Number
60-72	Mostek Part Number[2]
Second Card	
1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer
Third Card	
1-5	Mostek Part Number[2]
10-16	Organization[3]
29	A8[4]
30	A9[4]
31	A10[4]
32	Pull-up Resistor[5]
Fourth Card	
0-6	Data Format[4] — "MOSTEK"
15-28	Logic — "Positive Logic" or "Negative Logic"
35-57	Verification Code[7]
60-74	Package Choice[8]
Data Cards	
1-3	Decimal Address
5	Output B9
6	Output B8
7	Output B7
8	Output B6
9	Output B5
10	Output B4
11	Output B3
12	Output B2
13	Output B1
14	Output B0
16	Octal Equivalent of: B9[9]
17	Octal Equivalent of: B8, B7, B6[9]
18	Octal Equivalent of: B5, B4, B3[9]
19	Octal Equivalent of: B2, B1, B0[9]

Notes: 1. Positive or negative logic formats are accepted as noted in the fourth card.

2. Assigned by Mostek Marketing Department; may be left blank.

3. Punched as 0256x10.

4. A "0" indicates the chip is enabled by a logic 0, a "1" indicates it is enabled by a logic 1, and a "2" indicates a "Don't Care" condition.

5. A "1" indicates pull-ups; a "0" indicates no pull-ups.

6. "MOSTEK" format only is accepted on this part.

7. Punched as: (a) VERIFICATION HOLD — i.e. customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.

   (b) VERIFICATION PROCESS — i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification.

   (c) VERIFICATION NOT NEEDED — i.e. the customer will not receive a CVDS and production will begin immediately.

8. "24 PIN", "28 PIN STANDARD", or "28 PIN OPTIONAL" (left justified to column 60).

9. The octal parity check is created by breaking up the output word into groups of three from right to left and creating a base 8 (octal) number in place of these groups. For example the output word 1010011110 would be separated into groups 1/010/011/110 and the resulting octal equivalent number is 1236.

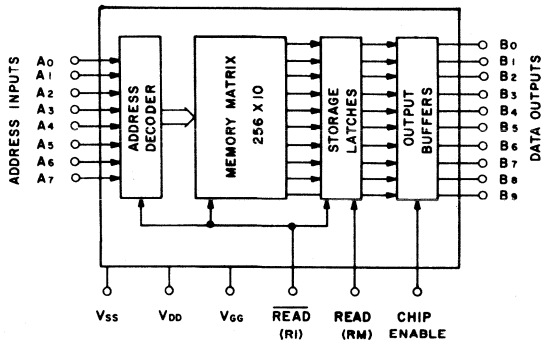
MK 2408 P

2560 Bit

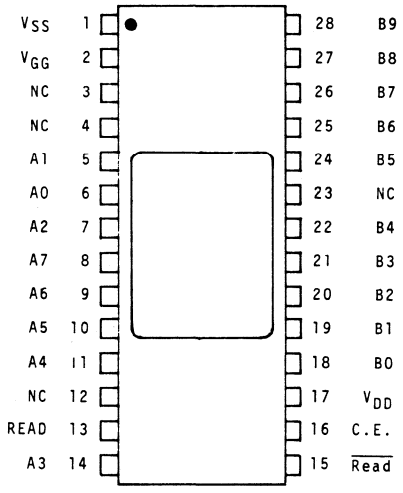
MOS Read-Only Memory Character Generator

MOSTEK

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



NC= NO CONNECTION

DESCRIPTION

The MK 2408 P is a pre-programmed member of the MK 2400 P Series. It is programmed as a dot-matrix character generator (64 characters) with ASCII encoded inputs and row (5-bit) outputs. The MK 2408 P outputs two rows at the same time. Row 1 is available at outputs B9 (left), B8, B7, B6, and B5 (right) while row 2 is available at outputs B4 (left), B3, B2, B1, and B0 (right). Row 3 is available at B9 through B5 while row 4 is available at B4 through B0. Row 5 and row 6 are available at B9 through B5 and B4 through B0. Row 5 and row 6 are available at B9 through B5 and B4 through B0. Row selection is determined by the address combination of bits A0 and A1.

The MK 2408 P meets and operates by the specifications outlined in the MK 2400 P Series data sheet (DS-24001270-2)

The example in Figure 1 demonstrates the correspondence of the device outputs and row select sequence to the 7 x 5 dot-matrix font. The complete character font patterns (truth table) are illustrated on the back. A logic 1 or a DOT represents an input or output voltage equal to V_{SS} (+5V) and a logic 0 or a blank represents a voltage equal to V_{DD} (OV). The eighth row outputs (B4 through B0 when inputs A1 and A0 equal logic 1) are not illustrated since in each case they are equal to all 0's.

A1	A0	B9 B4	B8 B3	B7 B2	B6 B1	B5 B0	
0	0	1	0	0	0	1	-- B9-B5
		1	1	0	1	1	-- B4-B0
0	1	1	0	1	0	1	-- B9-B5
		1	0	1	0	1	-- B4-B0
1	0	1	0	0	0	1	-- B9-B5
		1	0	0	0	1	-- B4-B0
1	1	1	0	0	0	1	-- B9-B5
		0	0	0	0	0	-- B4-B0

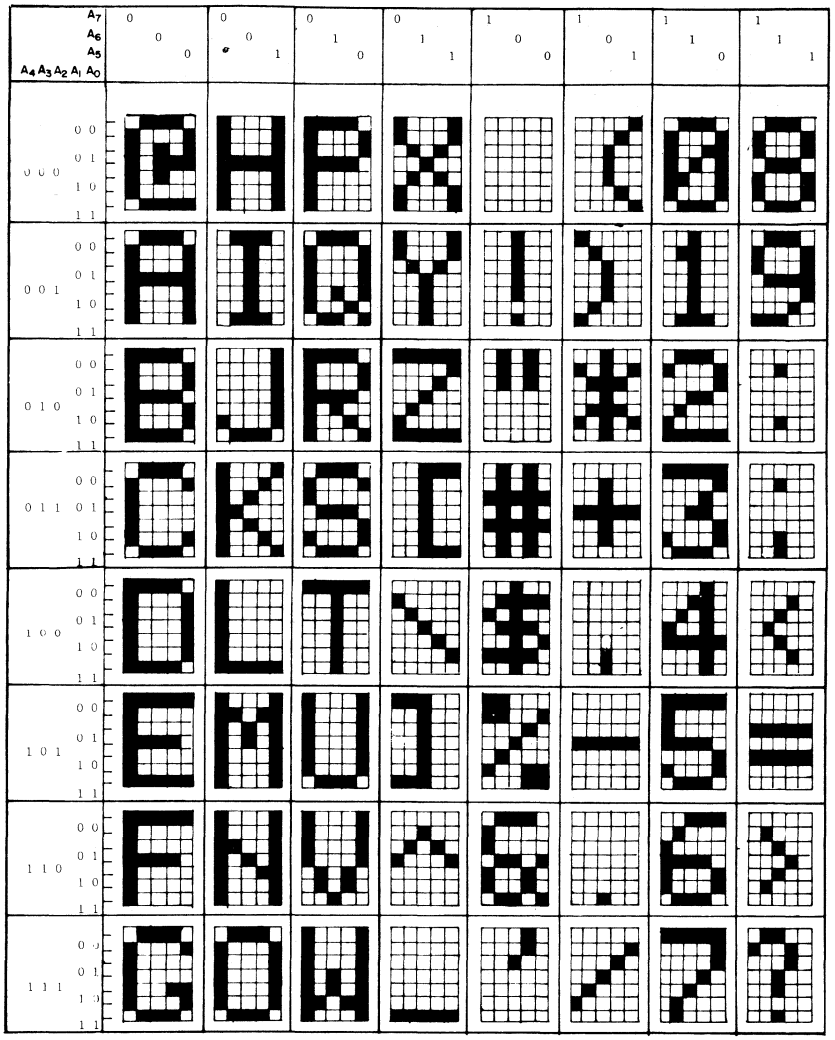
A7 = 0
A6 = 0
A5 = 1

A4 = 1
A3 = 0
A2 = 1

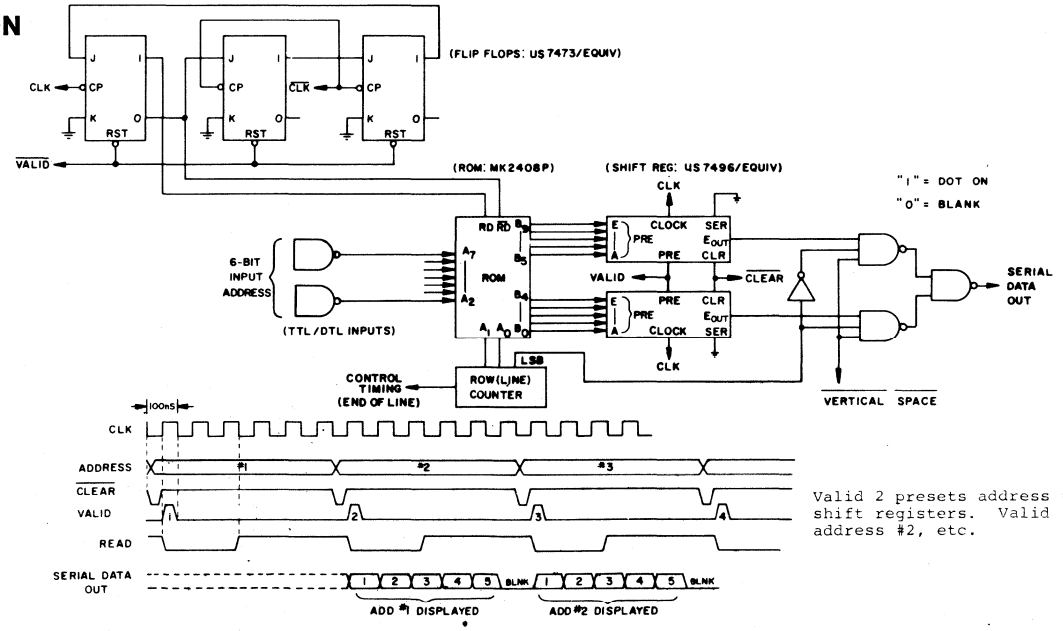
FIGURE 1

MOSTEK **MK2408P** **MOS Read-Only Memory Character Generator**

CODING & CHARACTER FONTS



APPLICATION



Valid 2 presets address #1 data in shift registers. Valid 3 presets address #2, etc.

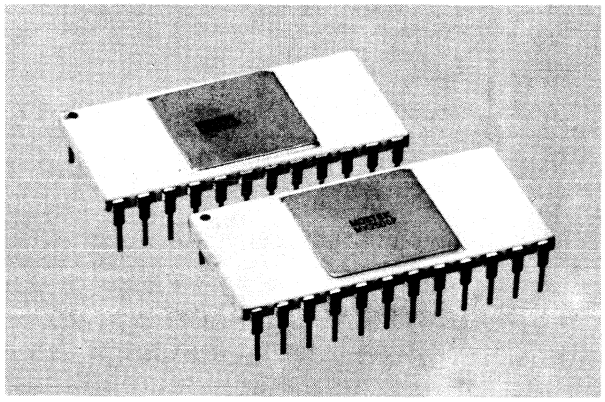
MK 2500 P
MK 2600 P

MOSTEK

4096-BIT
MOS Read-Only Memory

FEATURES

- ☐ High-speed, static operation — 400 nsec. typical access time
- ☐ Active input pull-ups provide worst-case TTL compatibility
- ☐ Push-pull outputs provide three output states: one, zero, and open
- ☐ Ion-implantation for constant current loads and lower power
- ☐ Standard power supplies: +5V, —12V
- ☐ MK 2500 P is pin-for-pin replacement for National 5232
- ☐ MK 2600 P is pin-for-pin replacement for Fairchild 3514



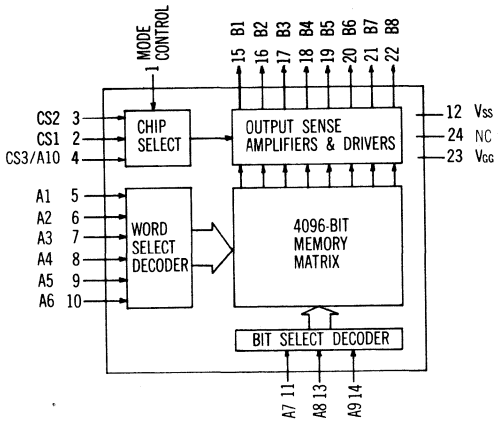
DESCRIPTION

The MK 2500 P and MK 2600 P series of TTL/DTL compatible MOS read-only memories (ROMs) are designed to store 4096 bits of information by programming one mask pattern. The word and bit organization of these ROM series is either 512W X 8B or 1024W X 4B.

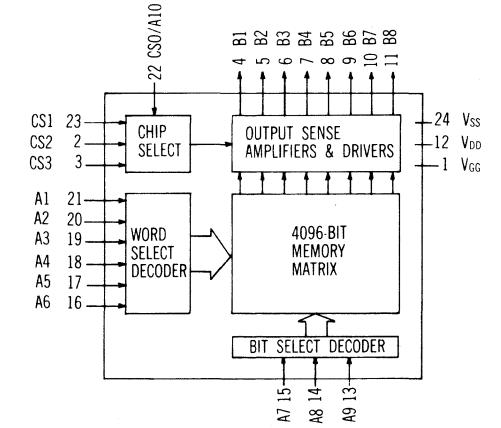
The MK 2500/2600 P series has push-pull outputs that can be in one of three states: logic one, logic zero, or open or unselected state. This, plus the programmable Chip Selects, enables the use of several ROMS in parallel with no external components. Since the ROM is a static device, no clocks are required, making the MK 2500/2600 P series of ROMS very versatile and easy to use.

Low threshold-voltage processing, utilizing ion-implantation, is used with P-channel, enhancement-mode MOS technology to provide direct input/output interfacing with TTL and DTL logic families. All inputs are protected to prevent damage from static charge accumulation.

FUNCTIONAL DIAGRAMS



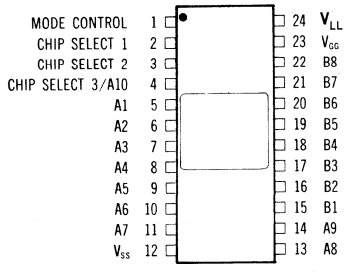
MK 2500P



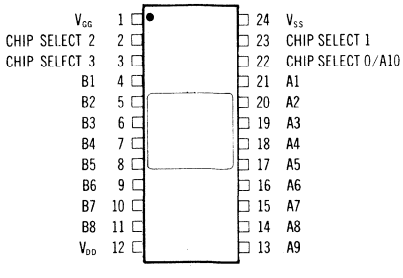
MK 2600 P

PIN CONNECTIONS

MK 2500 P



MK 2600 P



ABSOLUTE MAXIMUM RATINGS

Voltage on Any Terminal Relative to V_{SS} (except V_{GG}) ..... +0.3V to −10V
Voltage on V_{GG} Terminal Relative to V_{SS} ..... +0.3V to −20V
Operating Temperature Range (Ambient) ..... 0°C to +70°C
Storage Temperature Range (Ambient) ..... −55°C to +150°C

RECOMMENDED OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{SS}	Supply Voltage	+4.75	+5.0	+5.25	V	
V_{DD}	Supply Voltage	——	0.0	——	V	Note 1
V_{GG}	Supply Voltage	−11.4	−12.0	−12.6	V	
V_{IL}	Input Voltage, Logic "0"			+0.8	V	
V_{IH}	Input Voltage, Logic "1"	$V_{SS}-1.5$			V	Note 2
V_{IH}	Input Voltage, Logic "1"	2.4			V	Note 3

ELECTRICAL CHARACTERISTICS

($V_{SS} = +5.0V \pm 5\%$; $V_{DD} = 0$ V; $V_{GG} = -12V \pm 5\%$; $0°C \leq T_A \leq 70°C$ unless noted otherwise)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{SS}	Supply Current, V_{SS}		19.0	28.0	mA	Note 4
I_{GG}	Supply Current, V_{GG}		19.0	28.0	mA	Note 4
$I_{I(L)}$	Input Leakage Current, Any Input			10.0	μA	$V_I = V_{SS}-6.0V$. Note 2
I_{IL}	Input Current, Logic 0, Any Input			−100.0	μA	V_I=.4V. Note 3
I_{IH}	Input Current, Logic 1, Any Input			−600.0	μA	V_I=2.4V. Note 3
V_{OL}	Output Voltage, Logic "0"			0.4	V	I_{OL}=1.6mA
V_{OH}	Output Voltage, Logic "1"	2.4			V	$I_{OH}=-40\mu A$
$I_{O(L)}$	Output Leakage Current			+10	μA	Outputs disabled ($V_O=V_{SS}-6V$)
C_{IN}	Input Capacitance			10	pF	Note 5
C_O	Output Capacitance			10	pF	Note 5
t_{ACCESS}	Address to Output Access Time	100	400	700	nsec	Refer to
t_{CS}	Chip Select to Output Delay	100	250	500	nsec	Test
t_{CD}	Chip Deselect to Output Delay	100	250	800	nsec	Note 6 Circuit

Notes: 1. This is V_{LL} on MK 2500 P.

2. This parameter is for inputs without active pull-ups (programmable).

3. This parameter is for inputs with active pull-ups (programmable) for TTL interfaces. As the TTL driver goes to a logic 1 it must only provide 2.4V (this voltage must not be clamped) and the circuit pulls the input to V_{SS}. Refer to the Input pull-up figure for a graphical description of the active pull-up's operation.

4. Inputs at V_{SS}, outputs unloaded.

5. $V_{Bias} - V_{SS} = OV$; f = 1 MH_Z.

6. t_{CD} is primarily dependent on the RC time constant of the load (i.e. the outputs become open circuited upon being disabled). As noted in the Timing Diagram, disabling or enabling an output with a "1" expected out does not yield a transition through the 1.5V point; this is true because the TTL equivalent load pulls the open-circuited output to approximately 2 volts.

PROGRAMMING OPTIONS

MK 2500 P

	OPTIONS	
Function	512 X 8	1024 X 4
Mode Control	1	0
Chip Select 1	1 or 0	1 or 0
Chip Select 2	1 or 0	1 or 0
Chip Select 3/A10	1 or 0	address A10

1 = Most Positive = High Level Voltage

Pin 1 in the MK 2500 P is used as a Mode Control, setting the circuit in the 1024x4 or 512x8 mode. In the 1024x4 mode a tenth address bit is required, which is provided at Pin 4. If the circuit is in the 512x8 mode, then Pin 4 may be used for a third chip select.

Additional Options: The MK 2500 P can have the address and control inputs set by the user so that:

512x8: Mode Control — High
A10 — Low

1024x4: Mode Control — Low
A10 aid as an address
See Note 9, following page

MK 2600 P

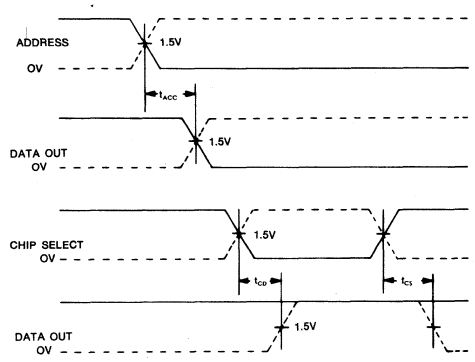
	OPTIONS	
Function	512 X 8	1024 X 4
Chip Select 0/A10	1 or 0	A10
Chip Select 1	1 or 0	1 or 0
Chip Select 2	1 or 0	1 or 0
Chip Select 3	1 or 0	1 or 0

1 = Most Positive = High Level Voltage

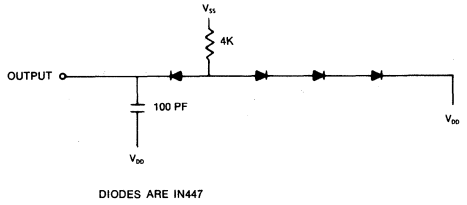
The MK 2600 P is programmed either as a 512x8 array or a 1024x4 array. In the 1024x4 arrays, Pin 22 provides the tenth address bit. When A10 is low the four bits are present at the even outputs (B2, B4, B6, and B8); when A10 is high, the bits are at the odd outputs (B1, B3, B5, and B7).

In 512x8 arrays, Pin 22 may be used to provide a fourth chip select. Thus, with four programmable chip selects, sixteen MK 2600 P ROMS in the 512x8 configuration can be arranged in an 8192x8 array requiring no external decoding.

TIMING

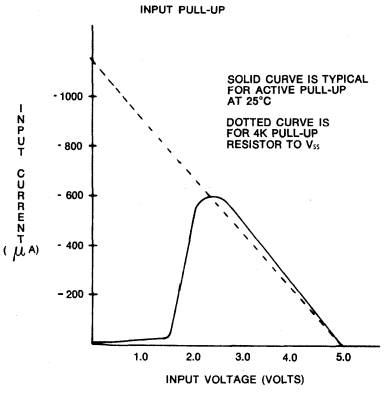


T_{ACCESS} TEST CIRCUIT

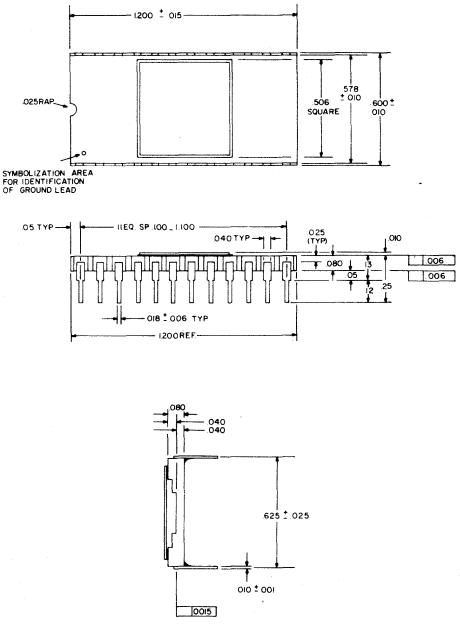


DIODES ARE IN447

INPUT



PACKAGE 24-lead ceramic dual-in-line hermatic



MOSTEK ROM PUNCHED-CARD CODING FORMAT[1]

MK 2500 P

First Card

Cols.	Information Field
1-30	Customer
31-50	Customer Part Number
60-72	Mostek Part Number[2]

Second Card

1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer

Third Card

1-5	Mostek Part Number[2]
10-16	Organization[3]
29	CS3[10]
30	CS2[4]
31	CS1[4]
32	Active Pull-ups[5]

Fourth Card

1-9	Data Format[6]
15-28	Logic — "Positive Logic" or "Negative Logic"
35-57	Verification Code[7]
60-67	"A10 EVEN" or "A10 ODD" (left justified)[9]

Data Cards/512x08 Organization

1-4	Decimal Address
6-13	Output B8- B1 (MSB thru LSB)
15-17	Octal Equivalent of output data[8]

Data Cards/1024x04 Organization

1-4	Decimal Address (0-1022), even addresses
6-9	Output (MSB-LSB)
11-12	Octal Equivalent of output data[8]
50-53	Decimal Address (1-1023), odd addresses
55-58	Output (MSB-LSB)
60-61	Octal Equivalent of output data[8]

MK 2600 P

First Card

Cols.	Information Field
1-30	Customer
31-50	Customer Part Number
60-72	Mostek Part Number[2]

Second Card

1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer

Third Card

1-5	Mostek Part Number[2]
10-16	Organization[3]
29	CS3[4]
30	CS2[4]
31	CS1[4]
32	CS0[10]
33	Active Pull-ups[5]

Fourth Card

1-9	Data Format[6]
15-28	Logic — "Positive Logic" or "Negative Logic"
35-57	Verification Code[7]

Data Cards/512x08 Organization

1-4	Decimal Address
6-13	Output B8- B1 (MSB thru LSB)
15-17	Octal Equivalent of output data[8]

Data Cards/1024x04 Organization

1-4	Decimal Address (0-1022), even addresses
6-9	Output (MSB-LSB)
11-12	Octal Equivalent of output data[8]
50-53	Decimal Address (1-1023), odd addresses
55-58	Output (MSB-LSB)
60-61	Octal Equivalent of output data[8]

Notes:

1. Positive or negative logic formats are accepted as noted in the fourtn card.
2. Assigned by Mostek Marketing Department; may be left blank.
3. Punched as "0512x08" or "1024x04".
4. A "0" indicates the chip is enabled by a logic 0, a "1" indicates it is enabled by a logic 1, and a "2" indicates a "Don't Care" condition.
5. A "1" indicates active pull-ups; a "0" indicates no pull-ups.
6. MOSTEK, Fairchild, or National Punched-Card Coding Format may be used. Specify which punched card format used by punching either "MOSTEK", "Fairchild", or "National". Start name at column one.
7. Punched as:
   (a) VERIFICATION HOLD — i.e. customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.
   (b) VERIFICATION PROCESS — i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification.
   (c) VERIFICATION NOT NEEDED — i.e. the customer will not receive a CVDS and production will begin immediately.
8. The octal parity check is created by breaking up the output word into groups of three from right to left and creating a base 8 (octal) number in place of these groups. For example the output word 10011110 would be separated into groups 10/011/110 and the resulting octal equivalent number is 236.
9. "A10 EVEN" and "A10 ODD" applies to the 1024 x 4 mode. "A10 EVEN" means the even outputs are enabled when A10 is high. "A10 ODD" means the odd outputs are enabled when A10 is high.
10. Punched as "2" for 1024 x 4 organization.

ASCII-TO-EBCDIC CODE CONVERTER
EBCDIC-TO-ASCII CODE CONVERTER

A_1 = LSB B_1 = LSB
A_9 = MSB B_8 = MSB

MK 2503 P

Function	512 X 8
Mode Control	1
Chip Select 1	0
Chip Select 2	0
Chip Select 3/A10	0

MK 2601 P

Function	512 X 8
Chip Select 0/A10	0
Chip Select 1	0
Chip Select 2	0
Chip Select 3	0

ASCII (ADDRESS) TO EBCDIC (DATA)

0 00000000	1 00000001	2 00000010	3 00000011	128 00100000	129 00100001	130 00100010	131 00100011
4 00110111	5 00101101	6 00101110	7 00101111	132 00100100	133 00010101	134 00000110	135 00010111
8 00010110	9 00000101	10 00100101	11 00001011	136 00101000	137 00101001	138 00101010	139 00101011
12 00001100	13 00001101	14 00001110	15 00001111	140 00101100	141 00001001	142 00001010	143 00011011
16 00010000	17 00010001	18 00010010	19 00010011	144 00110000	145 00110001	146 00011010	147 00110011
20 00111100	21 00111101	22 00110010	23 00100110	148 00110100	149 00110101	150 00110110	151 00001000
24 00011000	25 00011001	26 00111111	27 00100111	152 00111000	153 00111001	154 00111010	155 00111011
28 00011100	29 00011101	30 00011110	31 00011111	156 00000100	157 00010100	158 00111110	159 11100001
32 01000000	33 01001111	34 01111111	35 01111011	160 01000001	161 01000010	162 01000011	163 01000100
36 01011011	37 01101100	38 01010000	39 01111101	164 01000101	165 01000110	166 01000111	167 01001000
40 01001101	41 01011101	42 01011100	43 01001110	168 01001001	169 01010001	170 01010010	171 01010011
44 01101011	45 01100000	46 01001011	47 01100001	172 01010100	173 01010101	174 01010110	175 01010111
48 11110000	49 11110001	50 11110010	51 11110011	176 01011000	177 01011001	178 01100010	179 01100011
52 11110100	53 11110101	54 11110110	55 11110111	180 01100100	181 01100101	182 01100110	183 01100111
56 11111000	57 11111001	58 01111010	59 01011110	184 01101000	185 01101001	186 01110000	187 01110001
60 01001100	61 01111110	62 01101110	63 01101111	188 01110010	189 01110011	190 01110100	191 01110101
64 01111100	65 11000001	66 11000010	67 11000011	192 01110110	193 01110111	194 01111000	195 10000000
68 11000100	69 11000101	70 11000110	71 11000111	196 10001010	197 10001011	198 10001100	199 10001101
72 11001000	73 11001001	74 11010001	75 11010010	200 10001110	201 10001111	202 10010000	203 10011010
76 11010011	77 11010100	78 11010101	79 11010110	204 10011011	205 10011100	206 10011101	207 10011110
80 11010111	81 11011000	82 11011001	83 11100010	208 10011111	209 10100000	210 10101010	211 10101011
84 11100011	85 11100100	86 11100101	87 11100110	212 10101100	213 10101101	214 10101110	215 10101111
88 11100111	89 11101000	90 11101001	91 01001010	216 10110000	217 10110001	218 10110010	219 10110011
92 11100000	93 01011010	94 01011111	95 01101101	220 10110100	221 10110101	222 10110110	223 10110111
96 01111001	97 10000001	98 10000010	99 10000011	224 10111000	225 10111001	226 10111010	227 10111011
100 10000100	101 10000101	102 10000110	103 10000111	228 10111100	229 10111101	230 10111110	231 10111111
104 10001000	105 10001001	106 10010001	107 10010010	232 11001010	233 11001011	234 11001100	235 11001101
108 10010011	109 10010100	110 10010101	111 10010110	236 11001110	237 11001111	238 11011010	239 11011011
112 10010111	113 10011000	114 10011001	115 10100010	240 11011100	241 11011101	242 11011110	243 11011111
116 10100011	117 10100100	118 10100101	119 10100110	244 11101010	245 11101011	246 11101100	247 11101101
120 10100111	121 10101000	122 10101001	123 11000000	248 11101110	249 11101111	250 11111010	251 11111011
124 01101010	125 11010000	126 10100001	127 00000111	252 11111100	253 11111101	254 11111110	255 11111111

EBCDIC (ADDRESS) TO ASCII (DATA)

256 00000000	257 00000001	258 00000010	259 00000011	384 11000011	385 01100001	386 01100010	387 01100011
260 10011100	261 00001001	262 10000110	263 01111111	388 01100100	389 01100101	390 01100110	391 01100111
264 10010111	265 10001101	266 10001110	267 00001011	392 01101000	393 01101001	394 11000100	395 11000101
268 00001100	269 00001101	270 00001110	271 00001111	396 11000110	397 11000111	398 11001000	399 11001001
272 00010000	273 00010001	274 00010010	275 00010011	400 11001010	401 01101010	402 01101011	403 01101100
276 10011101	277 10000101	278 00001000	279 10000111	404 01101101	405 01101110	406 01101111	407 01110000
280 00011000	281 00011001	282 10010010	283 10001111	408 01110001	409 01110010	410 11001011	411 11001100
284 00011100	285 00011101	286 00011110	287 00011111	412 11001101	413 11001110	414 11001111	415 11010000
288 10000000	289 10000001	290 10000010	291 10000011	416 11010001	417 01111110	418 01110011	419 01110100
292 10000100	293 00001010	294 00010111	295 00011011	420 01110101	421 01110110	422 01110111	423 01111000
296 10001000	297 10001001	298 10001010	299 10001011	424 01111001	425 01111010	426 11010010	427 11010011
300 10001100	301 00000101	302 00000110	303 00000111	428 11010100	429 11010101	430 11010110	431 11010111
304 10010000	305 10010001	306 00010110	307 10010011	432 11011000	433 11011001	434 11011010	435 11011011
308 10010100	309 10010101	310 10010110	311 00000100	436 11011100	437 11011101	438 11011110	439 11011111
312 10011000	313 10011001	314 10011010	315 10011011	440 11100000	441 11100001	442 11100010	443 11100011
316 00010100	317 00010101	318 10011110	319 00011010	444 11100100	445 11100101	446 11100110	447 11100111
320 00100000	321 10100000	322 10100001	323 10100010	448 01111011	449 01000001	450 01000010	451 01000011
324 10100011	325 10100100	326 10100101	327 10100110	452 01000100	453 01000101	454 01000110	455 01000111
328 10100111	329 10101000	330 01011011	331 00101110	456 01001000	457 01001001	458 11101000	459 11101001
332 00111100	333 00101000	334 00101011	335 00100001	460 11101010	461 11101011	462 11101100	463 11101101
336 00100110	337 10101001	338 10101010	339 10101011	464 01111101	465 01001010	466 01001011	467 01001100
340 10101100	341 10101101	342 10101110	343 10101111	468 01001101	469 01001110	470 01001111	471 01010000
344 10110000	345 10110001	346 01011101	347 00100100	472 01010001	473 01010010	474 11101110	475 11101111
348 00101010	349 00101001	350 00111011	351 01011110	476 11110000	477 11110001	478 11110010	479 11110011
352 00101101	353 00101111	354 10110010	355 10110011	480 01011100	481 10011111	482 01010011	483 01010100
356 10110100	357 10110101	358 10110110	359 10110111	484 01010101	485 01010110	486 01010111	487 01011000
360 10111000	361 10111001	362 01111100	363 00101100	488 01011001	489 01011010	490 11110100	491 11110101
364 00100101	365 01011111	366 00111110	367 00111111	492 11110110	493 11110111	494 11111000	495 11111001
368 10111010	369 10111011	370 10111100	371 10111101	496 00110000	497 00110001	498 00110010	499 00110011
372 10111110	373 10111111	374 11000000	375 11000001	500 00110100	501 00110101	502 00110110	503 00110111
376 11000010	377 01100000	378 00111010	379 00100011	504 00111000	505 00111001	506 11111010	507 11111011
380 01000000	381 00100111	382 00111101	383 00100010	508 11111100	509 11111101	510 11111110	511 11111111

PRELIMINARY

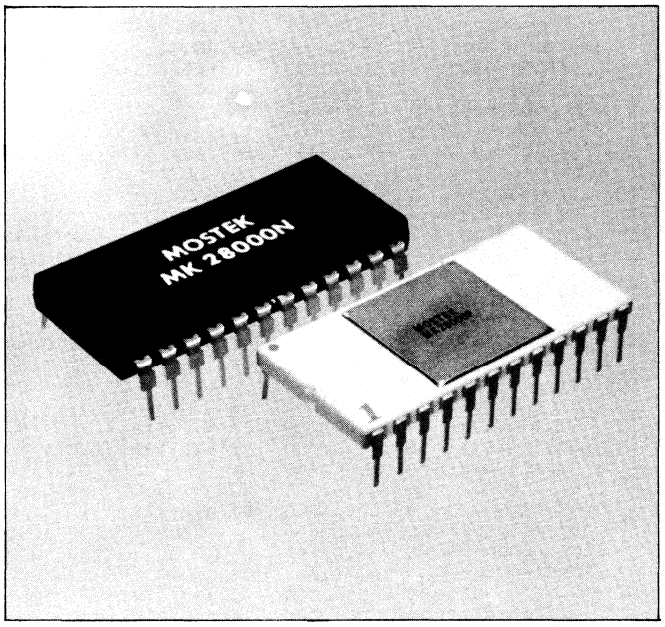
MK 28000N
MK 28000 P

16K-BIT
MOS Read-Only Memory

MOSTEK

FEATURES:

- ☐ 600 ns Maximum Access Time
- ☐ Low Power Dissipation
  Active — 0.02 mW/bit Typ.
  Inactive — .007 mW/bit Typ.
- ☐ EA 4900 and EA 4800 Pin-for-pin Replacement
- ☐ 2K x 8 or 4K x 4 organization with Open Drain Outputs
- ☐ Standard Supplies +5 volts, — 12 volts
- ☐ Ion-Implanted for Full TTL/DTL Compatibility



DESCRIPTION:

The MK 28000 is a mask programmable read only memory utilizing low-threshold Ion-Implant, P-Channel technology. The MK 28000 is a pin-for-pin replacement for the EA 4900. The MK 28000 may be organized as either a 2K x 8 or 4K x 4 memory.

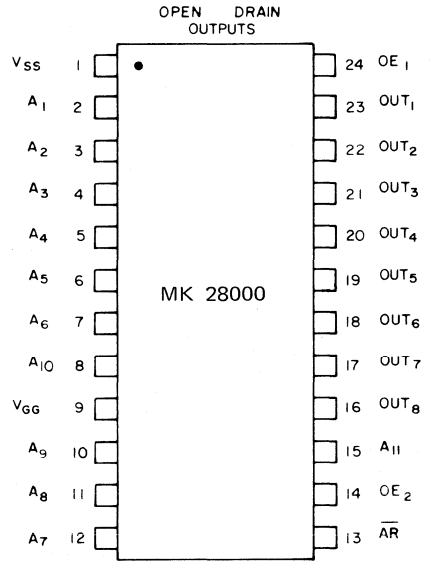
The MK 28000 open drain outputs are divided into two groups with one Output Enable line controlling each group of outputs. This feature allows the MK 28000 to be either a 2K x 8 or a 4K x 4 memory without any internal mask changes. For a 2K x 8 organization, the Output Enables (OE_1, OE_2) are tied together. For a 4K x 4 organization, the four outputs associated with OE_1 are wire-ORed to the four outputs associated with OE_2. OE_1 and OE_2 are inverted with respect to each other and used as the twelfth address input in the 4K x 4 organization.

The internal circuitry of the MK 28000 is dynamic. This features means low standby power consumption when the ROM is not being addressed.

All inputs are protected against static charge accumulation. Pullup resistors on all inputs are available as a programmable option.

With no address lead time required, system design is simplified; address and $\overline{AR}$ may appear simultaneously.

PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Voltage on any terminal relative to V_{SS} . . . . . +0.3V to −20V

Operating temperature range (Ambient). . . . . 0°C to 70°C

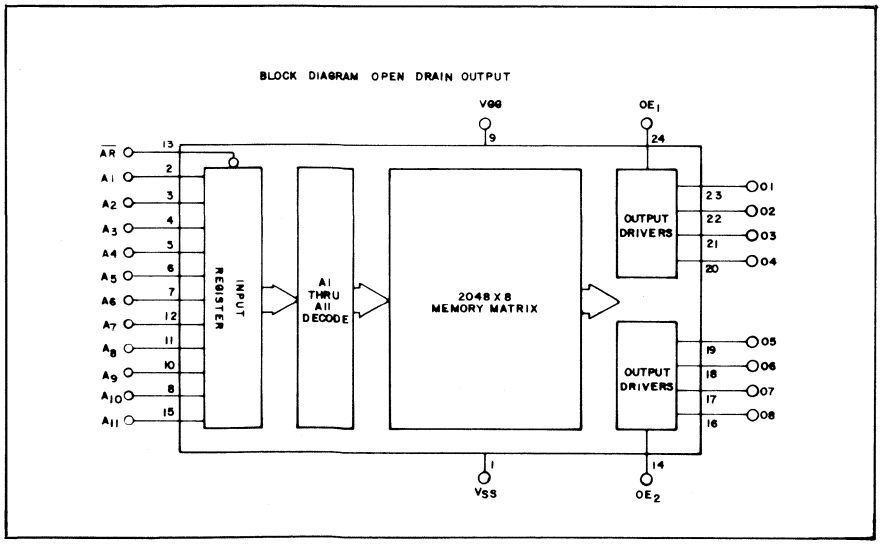
Storage temperature range (Ambient) . . . . . −55°C to 150°C

	PARAMETER	MIN	TYP	MAX	COMMENTS
V_{SS}	Supply Voltage	+4.75V	+5V	+5.25V	
	TTL Reference	—	0	—	
V_{GG}	Supply Voltage	−12.6V	−12V	−11.4V	
V_{IL}	Input Voltage, Logic "0"	V_{GG}		+.8V	
V_{IH}	Input Voltage, Logic "1"	V_{SS} − 1.5V		V_{SS}	Pullup resistors to V_{SS} (≈5K) available as an option

ELECTRICAL CHARACTERISTICS

(V_{SS} = +5.0V ±5%; V_{DD} = 0V; V_{GG} = −12V ±5%; 0°C ≤ T_A ≤ 70°C)

	PARAMETER	MIN	TYP	MAX	COMMENTS
I_{SS}	Supply Current		20 mA	30 mA	See Note 1
I_{GG}	Supply Current		−20 mA	−30 mA	Inputs at V_{SS}
I_{GG}	Supply Current (Standby)		7 mA	12 mA	See Note 1
C_{IN}	Input Capacitance (Address & OE's)		8 pF	10 pF	See Note 2
C_{IN}	Input Capacitance ($\overline{AR}$)		12 pF	15 pF	See Note 2
I_{IN}	Input Leakage			10 µA	See Note 3
R_{IN}	Input Pullup Resistors	3 KΩ		11 KΩ	Optional
V_{OH}	Output Voltage, Logic "1"	2.4V			See Note 4
I_{OL}	Output Leakage Current	−10 µA		+10µA	V_O = V_{SS} −6V, T_A = 25°C (outputs disabled)

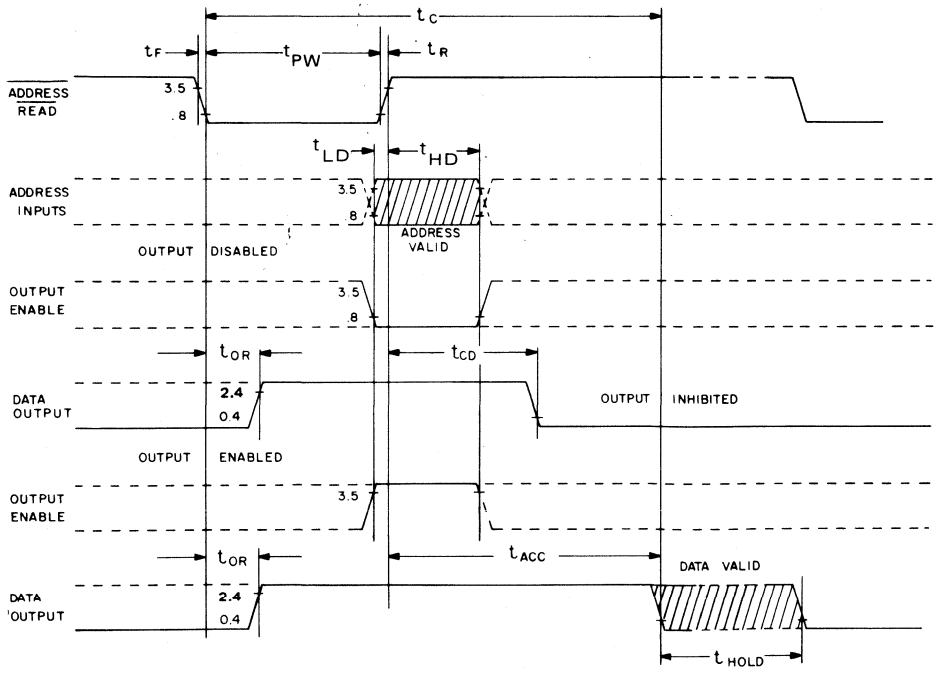


	PARAMETER	MIN	TYP	MAX	COMMENTS
t_{PW}	$\overline{AR}$ Precharge Time	400 ns		∞	
t_C	Cycle Time	1 µs + t_R + t_F			t_{ACC} + t_{PW} + t_R + t_F
t_{ACC}	Access Time			600 ns	See note 4
t_{LD}	Address Lead Time	0			
t_{HD}	Address Hold Time	250 ns			
t_R	$\overline{AR}$ Rise Time			100 ns	
t_F	$\overline{AR}$ Fall Time			100 ns	
t_{HOLD}	Data Output Valid Time	100 µs			See note 5
t_{CD}	Output Disable Time			300 ns	See note 4
t_{OR}	Output Reset Time	75 ns		400 ns	See note 4

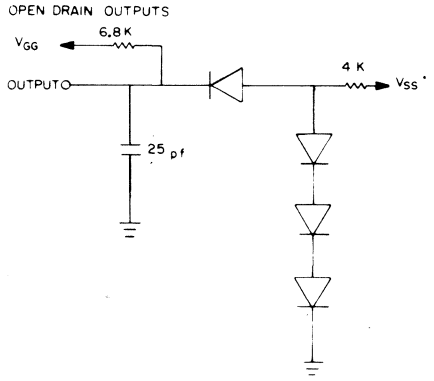
NOTES:

1. Outputs disconnected with no internal pullup resistors.
2. $V_{BIAS} - V_{SS} = 0V$; f = 1 MHz
3. This parameter is for inputs without pullups (optional)
4. With test circuit shown below
5. or, until the next precharge + t_{OR}

TIMING



TEST CIRCUIT



MOSTEK 28000 ROM Punched Card Coding Format[1]

First Card

Cols	Information Field
1-30	Customer
31-50	Customer Part Number
60-72	MOSTEK Part Number[2]

Second Card

1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer

Third Card

1-5	MOSTEK Part Number[2]
33	Input Pullups (1=yes, 0=no)

Fourth Card

1-9	Data Format[3]
15-28	Logic – ("Positive Logic" or "Negative Logic")
35-57	Verification Code[4]

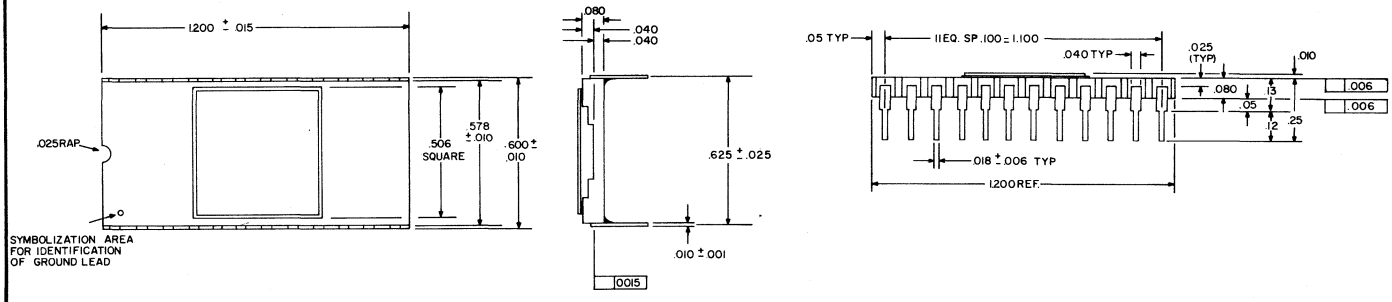
Data Cards

MOSTEK Format or EA Format

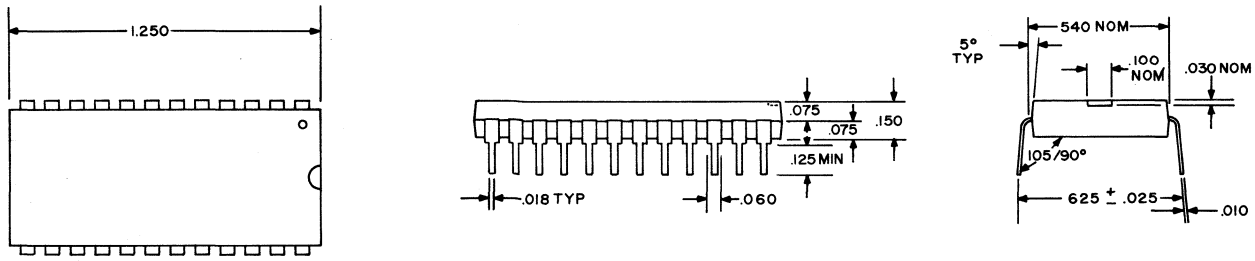
1-4	Decimal Address
6-13	Output 08-01 (MSB Thru LSB)
15-17	Octal Equivalent of Output Data

NOTES:
1. Positive or negative logic formats are accepted as noted in the fourth card.
2. Assigned by MOSTEK; may be left blank.
3. MOSTEK or Electronic Arrays Punched card coding format may be used. Specify which card format used by punching either "MOSTEK" or "EA". Start at column one.
4. Punches as:
   (a) VERIFICATION HOLD – i.e. customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.
   (b) VERIFICATION PROCESS – i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification
   (c) VERIFICATION NOT NEEDED – i.e. the customer will not receive a CVDS and production will begin immediately.

PACKAGE DESCRIPTION 24-pin Dual-in-Line Ceramic



PACKAGE DESCRIPTION 24-pin Dual-in-Line Plastic



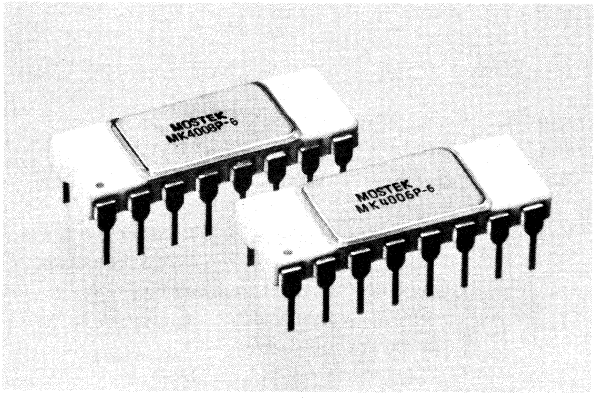
MK 4006 P-6
MK 4008 P-6

1024x1 BIT DYNAMIC
MOS Random Access Memory

MOSTEK

FEATURES:

- ☐ TTL/DTL compatible inputs
- ☐ No clocks required
- ☐ Access time:
  MK 4006 P–6 under 400 ns
  MK 4008 P–6 under 500 ns
- ☐ Standby power: under 50 mW
- ☐ 16-pin standard CDIP
- ☐ Supply voltage: +5V and −12V



DESCRIPTION

This is a family of MOS dynamic 1024x1 random-access memories having identical functional characteristics, differing only in speed. Access time in the MK 4006 P-6 is less than 400 ns; in the MK 4008 P-6 less than 500.

Full address decoding is provided internally. Information is read out non-destructively (NDRO) and has the same polarity as the input data.

TTL/DTL compatibility at all inputs allows economical use in small systems by eliminating the need for special interface circuitry. Large main-memory applications also benefit from the low drive-voltage swings as well as the packing density afforded by the standard 16-pin dual-in-line packaging and low standby power.

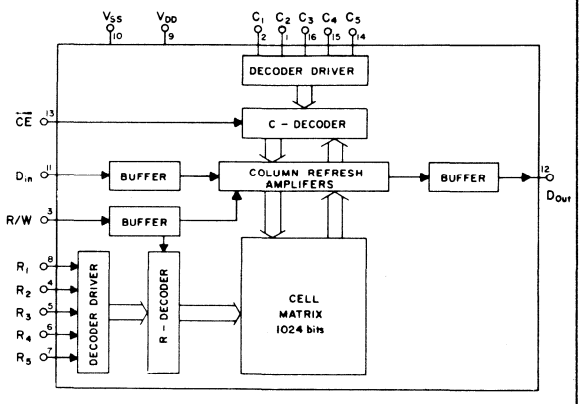
The internal memory element of this RAM is a capacitance, and refreshing must be periodically initiated (see TIMING). However, all internal decoding and sensing is static, so that precharging or clocking normally associated with dynamic memories is not required. From the user's viewpoint, memory control and addressing are essentially those of a static device.

Noise suppression measures normally employed in DTL or TTL systems are sufficient. High voltage input swings and high peak-current line drivers are unnecessary for driving memory inputs, and the memory itself does not exhibit large supply current transients.

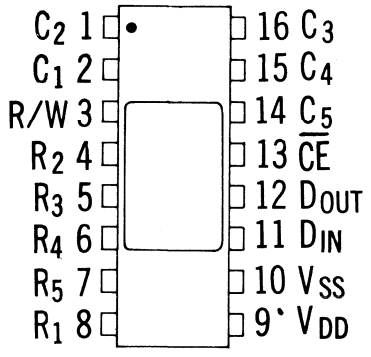
Data output is single-ended to minimize propagation delay. Output current is sourced from V_{SS} (+5V), and easily sensed using readily available components. A logic 1 at the output terminal appears as a 5,000 Ohm resistor (MK 4006) to +5V; a logic 0 as an open circuit.

The performance of this RAM is made possible by Mostek's ion-implantation process. In addition to offering low threshold voltages for TTL/DTL compatibility and utilizing conventional P-channel processing, ion-implantation allows both enhancement (normally OFF) and depletion (normally ON) MOS transistors to be fabricated on the same chip. By replacing conventional MOS load resistors with constant-current depletion transistors, operational speeds and functional density are increased.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} ..... +0.3 to −20V
Operating Temperature ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C

RECOMMENDED DC OPERATING CONDITIONS

(0° C $\leq T_A \leq$ 70°C)

	PARAMETER	MK 4006P-6 MIN	MK 4006P-6 MAX	MK 4008P-6 MIN	MK 4008P-6 MAX	UNITS	NOTES
V_{SS}	Supply Voltage		+4.75		+5.25	V	
V_{DD}	Supply Voltage		−11.4		−12.6	V	
V_{IL}	Input Voltage, Logic 0				+0.8	V	
V_{IH}	Input Voltage, Logic 1		$V_{SS}-1$		V_{SS}	V	
V_{SB}	Standby Supply Voltage (Fig. 4)		$V_{SS}-4$		$V_{SS}-6$	V	Note 1

RECOMMENDED AC OPERATING CONDITIONS[2]

(0° C $\leq T_A \leq$ 70°C)

	PARAMETER	MK 4006P-6 MIN	MK 4006P-6 MAX	MK 4008P-6 MIN	MK 4008P-6 MAX	UNITS	NOTES
t_{RC}	Read Cycle Time (Fig. 1)	400		500		ns	
t_{WC}	Write Cycle Time (Fig. 2)	650		900		ns ns	t_{WP}=250 ns t_{WP}=400 ns
t_{WP}	Write Pulse Width (Fig. 2)	250		400		ns ns	t_{AW}=400 ns t_{AW}=500 ns
t_{AW}	Address-to-Write Delay (Fig. 2)	400		500		ns ns	t_{WP}=250 ns t_{WP}=400 ns
t_{DLD}	Data-to-Write Lead Time (Fig. 2)	300		400		ns ns	t_{WP}=250 ns t_{WP}=400 ns
t_{RDLY}	Refresh Time (Fig. 3)		2		2	ms	See Note 3.
t_{CDPD}	Chip-Disable-to-Power-Down Delay (Fig. 4)	200		200		ns	See Note 1 See Note 4

DC ELECTRICAL CHARACTERISTICS

(V_{SS} = +5V ± 5%; V_{DD} = −12V ± 5%; 0°C $\leq T_A \leq$ 70°C unless otherwise noted)

	PARAMETER	MK 4006P-6 MIN	MK 4006P-6 MAX	MK 4008P-6 MIN	MK 4008P-6 MAX	UNITS	NOTES
I_{SS}, I_{DD}	Supply Current: At T_A=0°C		32		32	mA	Output
	At T_A=70°C		27		27	mA	Open
P_{SDBY}	Power Dissipation, Standby		50		50	mW	$V_{SS}-V_{DD}$ = 5V; Note 1
I_{IH}	Input Current, Logic 1. Any Input	−5	+5	−5	+5	μA	$V_I=V_{SS}-1V$
I_{IL}	Input Current, Logic 0, Any Input	−5	+5	−5	+5	μA	V_I=0.8V
I_{OH}	Output Current, Logic 1	1.0		0.8		mA	Note 5
I_{OL}	Output Current, Logic 0		5		5	μA	

AC ELECTRICAL CHARACTERISTICS

(V_{SS} = +5V ± 5%; V_{DD} = −12V ± 5%; 0°C ≤ T_A ≤ 70°C unless otherwise noted)

	PARAMETER	MK 4006P-6 MIN	MK 4006P-6 MAX	MK 4008P-6 MIN	MK 4008P-6 MAX	UNITS	NOTES
t_{ACCESS}	Read Access Time (Fig. 1 & 1-A)		400		500	ns	Note 2
t_{CE}	Chip Enable Time (Fig. 1A & 5)		350		450	ns	Note 2
t_{CD}	Chip Disable Time (Fig. 1A & 5)		350		450	ns	
C_I	Input Capacitance, Any Input		5.0		5.0	pF	T_A=25°C; V_I=V_{SS}; f=1MHz
C_O	Output Capacitance		10		10	pF	T_A=25°C; V_O=V_{SS}−5V; f=1MHz
C_{DD}	V_{DD} Capacitance		75		75	pF	T_A = 25°C; Note 6

NOTES:

(1) Applies to MK 4006-6 and MK 4008-6 only.

(2) Measurement Criteria: Input voltage swing, all inputs: 0.8V to V_{SS} — 1
Input rise and fall times: 20 ns
Measurement point on input signals: +1.5V above ground
Measurement point on output signal: +60 mV above ground, using a load circuit of a 200 ohm resistor in parallel with a 100 pF capacitance connected to ground.

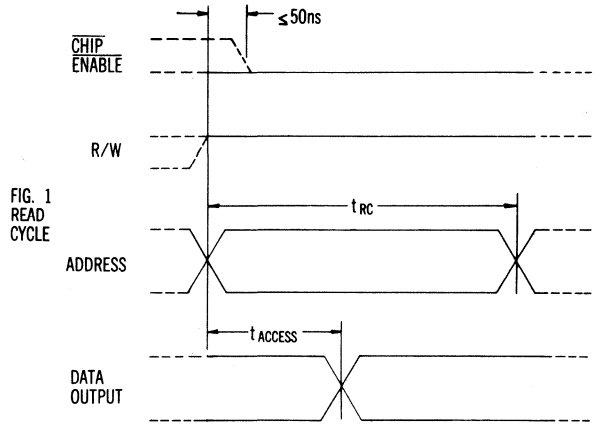
(3) t_{RDLY} is the time between refresh cycles for a given row address.

(4) The rise time of V_{DD} must not be faster than 20 ns.

(5) Steady-state values. (Refer to Fig. 1A for clarification)

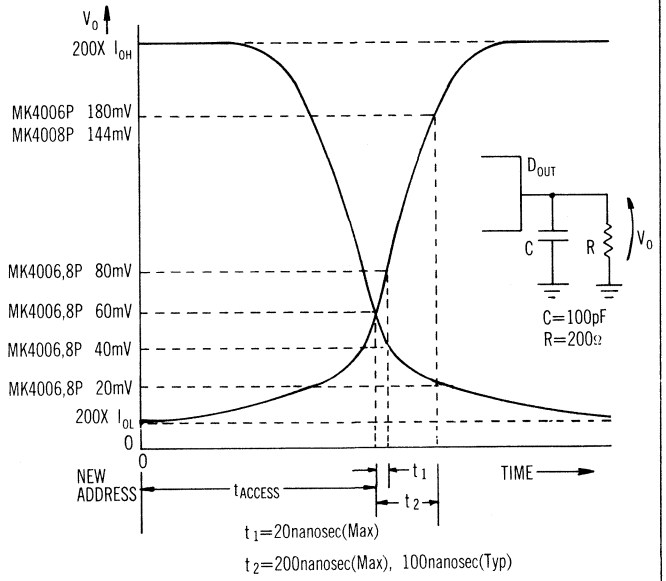
(6) Average capacitance of the V_{DD} terminal relative to the V_{SS} terminal. Measured by switching the V_{DD} terminal from OV to —12V with an applied V_{SS} = 5V. Peak I_{DD} is observed and the circuit replaced by a capacitance which yields the same peak current as the circuit under test.

TIMING (Note 2)



READING (Fig. 1)

Reading is accomplished with the Read/Write input held high. Data output directly follows the application of an address. As long as the address is unchanged and the chip enabled, data output will remain valid until the next refresh cycle. Input addresses can be changed as soon as output data is accessed. Any address can be applied repetitively without degrading stored data, providing that the refresh period of 2 ms is observed.



ACCESS TIME (Fig. 1-A)

Figure 1-A illustrates the measurement of access time after application of new address for the MK 4006 P and the MK 4008 P.

TIMING
(Note 2)

WRITING (Fig. 2)

Writing is accomplished by bringing the Read/Write input low with valid data present at the data input and the Chip-Enable input low (chip enabled). Following the return of the Read/Write line to a high state, new address and input data can be applied. If a read-after-write operation is desired, valid data will appear at the output within one read access time following the rising edge of the Write Pulse. Read-modify-write operation is easily achieved by delaying the Write Pulse until data has been read and modification is complete.

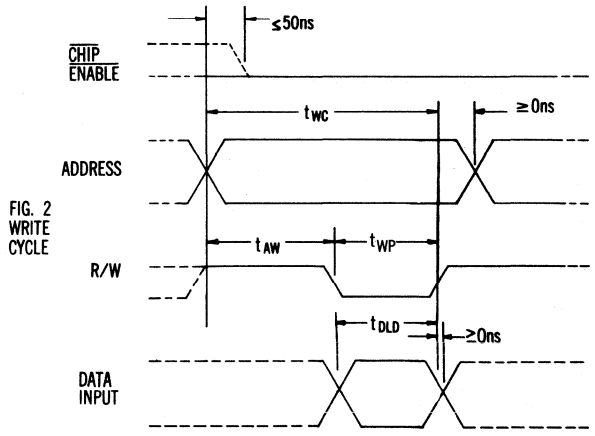


FIG. 2 WRITE CYCLE

REFRESHING (Figs. 2 & 3)

The dynamic memory cell employed in the MK 4006 P and MK 4008 P will not store data indefinitely. Stored data must be written back into the cell at least once every 2 ms. Rewriting is accomplished internally without the need to reapply external data. This rewriting operation is called *refreshing.*

Refreshing of the MK 4006 P and MK 4008 P is accomplished during both *write cycles* and *refresh cycles.* During a write cycle the state of the Row Address (R_1-R_5) determines which of the 32 memory matrix rows will be internally refreshed. An entire row (32 bits) is refreshed during one write cycle. Since it is difficult in practice to assure that each of the 32 possible R addresses is associated with a write cycle in every 2 ms period, a separate refresh cycle is normally employed.

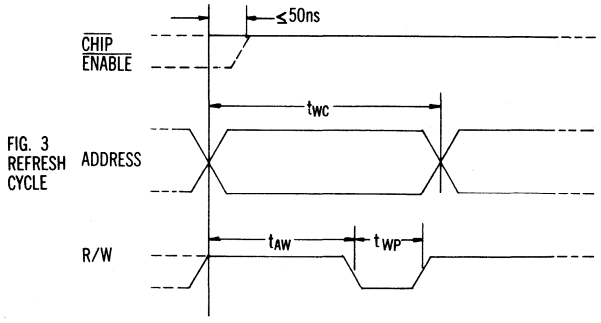


FIG. 3 REFRESH CYCLE

The refresh cycle is identical to the write cycle except that the chip is disabled while the Read/Write line is pulsed. Disabling the chip removes the data output and prevents data at the data input from being written into the memory. An entire refresh cycle consists of 32 address changes and associated write pulses, involving a total time of approximately 20 microseconds.

STANDBY MODE (Fig. 4)

Power dissipation of the MK 4006-6 P and MK 4008-6 P can be reduced below 50 mW without loss of stored data by lowering the V_{DD} supply voltage to system ground (V_{SS}-5V). Figure 4 illustrates the proper input conditions that should be observed when reducing V_{DD}. If the standby mode is maintained as long as 2 milliseconds, the V_{DD} supply should be returned to −12V and a refresh cycle initiated. Read or write cycles can commence immediately following the return of V_{DD} to −12V.

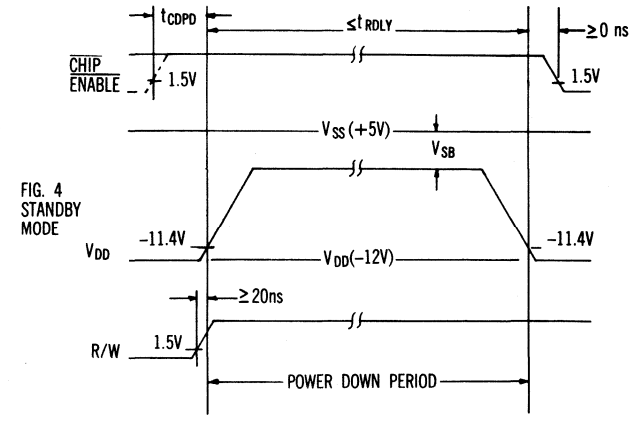


FIG. 4 STANDBY MODE

TIMING
(Note 2)

CHIP ENABLING (Fig. 5)[1]

The negative-going $\overline{CE}$ enables the chip, and output data becomes valid within t_{CE} time. Return of the $\overline{CE}$ input to logic 1 disables the chip; data out remains for t_{CD} time.

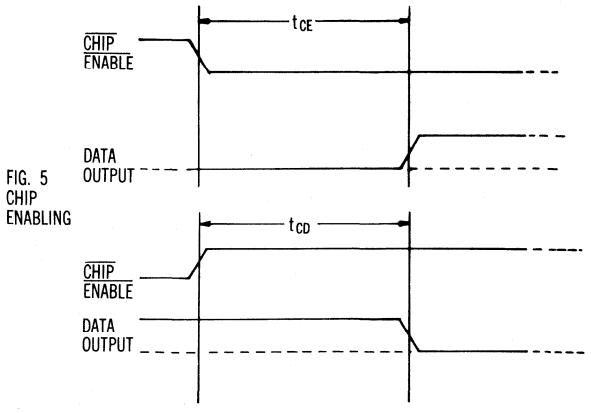


FIG. 5 CHIP ENABLING

TESTING CONSIDERATIONS

For a complete discussion of testing this memory, see Mostek's Applications Note AN-103.

The functional diagram (Fig. 6) indicates signal flow for selected row and column.

A simplified listing of functional tests is shown in Table 1. (high = Logic 1; low = Logic 0)

Tests are performed in an address sequence which requires the maximum number of changes in the row and column decoders between addresses. Addressing Rows 0 through 31 is accomplished by using the binary equivalent of the row address. The internal organization of the memory matrix requires the logic shown in Fig. 7 for column addresses; this logic provides the necessary conversion from inary equivalent to column address.

Fig. 6

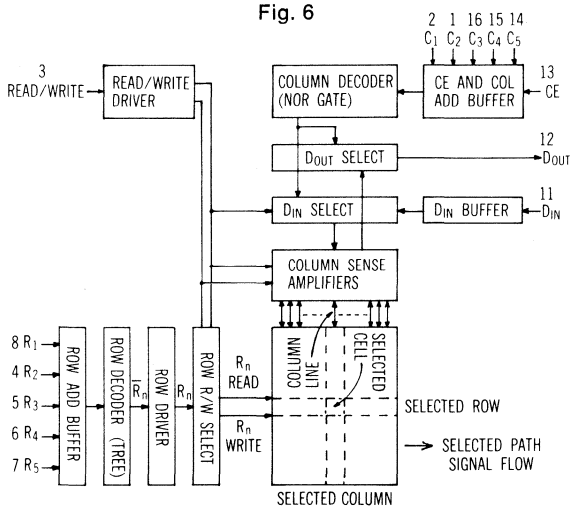


Fig. 7

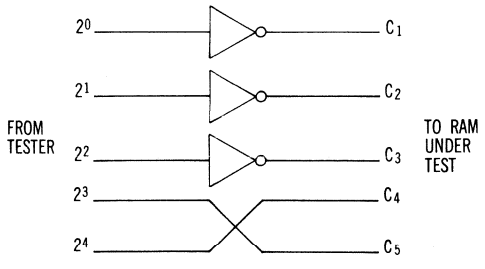
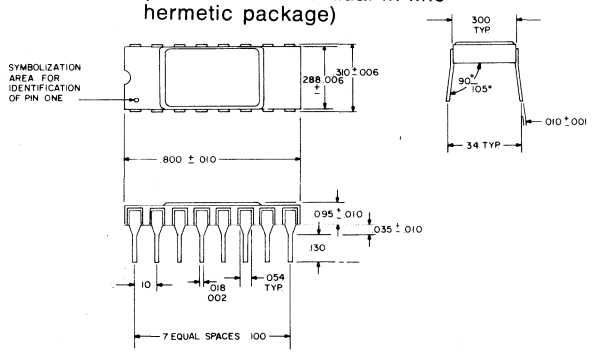


TABLE 1: FUNCTIONAL TESTS (SIMPLIFIED)

TEST DESC.	TEST SEQ.	OPER.	CHIP ENABLE	DATA INPUT	COMPARE DATA
Bit & Decoder Test[1]	First	Write	E	Parity	
	Next	Read	E		Parity
Column Shorts & No Write During Disable	First	Write	E	V-Bar	
	Next	Write	D	$\overline{\text{V-Bar}}$	
	Next	Read	E		V-Bar
Row Shorts, No Read During Disable, & Max. Power	First	Write	E	H-Bar	
	Next	Read	D	1	0
	Next	Read	E	0	H-Bar
Access Time, Refresh, Write Cycle, & Standby[1]	First	Write, Write	E	V-Bar, $\overline{\text{V-Bar}}$	
	Next	Delay	D	0	
	Next	Read	E		$\overline{\text{V-Bar}}$
Disturb Test	First	Write Row of 1's	E	1	
	Next	Write Adj. Row with 0's	E	0	
	Next	Continue Writing Same Row for Max. Refresh Delay	E	0	
	Next	Read original Row of 1's	E		1

1. Test performed as shown and repeated with complementary data.

PACKAGE (16-lead ceramic dual-in-line hermetic package)



ORDERING INFORMATION

MK 4006 P-6 1024x1 RAM/w/400 ns access time with power down
MK 4008 P-6 1024x1 RAM/w/500 ns access time with power down

APPLICATION

SENSE AMPLIFIERS FOR MK 4006/4008 RAM's

Since the interface circuitry used to convert memory signals to system logic levels strongly influences system access times, this circuitry should always be designed to meet the speed and cost requirements of the particular application.

Fig. 1-A (See "Timing") is shown to assist in the design of such amplifiers. This figure shows output voltage (across a specified load) vs. time from application of new address with several points indicated where specified voltage levels are referenced to specific times. Although all the various access times vs. output current levels cannot be shown, a few guidelines are given for interpolation between the specified points.

In Fig. 1-A, the two points at t_{access} + 20 nsec give the minimum "1" level and the maximum "0" level for this particular time (80 mV and 40 mV respectively). At t_{access} + 200 nsec, voltage levels are specified for the 90% and 10% points of the minimum "1" and maximum "0" levels.

INTERPOLATION

These interpolation guidelines are selected to give the designer a high level of confidence in his sense amplifier design.

From O to 1: This portion of the access curve can be estimated by two linear portions: (1) from the 60 mV to the 80 mV level; and (2) from the 80 mV level to 180/144 mV level.

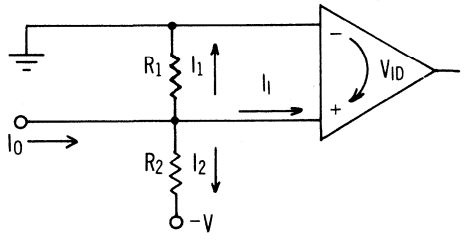
From 1 to O: This portion of the access curve can be estimated by a semi-logarithmic plot decreasing 20 mV for each decade or 10 nsec of time added to t_{access}, with the end points being 60 mV at 2 nsec and 20 mV at 200 nsec.

EXAMPLE: Let us consider how this data can be used in a sense amplifier design utilizing the 75107/108 Dual-Line-Receiver-and-Driver.

The manufacturer's data sheet for this circuit shows us that at strobe time, three conditions of the line receiver can exist: (1) the input voltage differential can be more positive than 25 mV, resulting in a logic 1 at the output (Input differential voltage is referenced to the inverting terminal); (2) the input differential can be more negative than 25 mV, resulting in a logic O at the output; (3) the input differential is less than 25 mV (absolute value), which will result in an output of an undetermined state. In other words, the line receiver has a 50 mV "window" centered around zero, and a signal must fall outside this window to provide reliable information at the output.

The standard configuration for using the 75107/108 as a sense amp is shown in Fig. 8 with the voltage and current conventions used in this analysis.

FIG. 8: Illustrating use of 75107/108 Line Receivers as sense amplifiers for the MK 4006/4008 P.



From the worst-case access at the *chip* level, one can use the interpolation technique described above to determine maximum "O" current level [I_{OLC}(MAX)] and the minimum "1" current level [I_{OH}(MIN)].

However, to use a worst-case approach to this design, in addition to the chip's characteristics, one must include in the "O" level current the effect of leakage from all outputs that are wired together. Also the input currents required by the 75107/108 (75 mA and 10 mA) must be included. Let us call this I_{OLT}(MAX):

$$I_{OLT}(MAX) = I_{OLC}(MAX) + (N\text{-}1)\ (5\ \mu A) \quad [1]$$

where N = number of outputs wired together

Using the maximum zero level at the line receiver input ($V_{ID} \leq -25mV = V_{ID}^{-}$), the following equation is derived:

$$I_{OLT}(MAX) = I_1 - I_2 + I_{IL}(MIN)$$

and $I_{IL}(MIN) = O\ \mu A$ [2]

therefore:

$$I_{OLT}(MAX) = \frac{V_{ID}^{-}}{R1} + \frac{V + V_{ID}^{-}}{R2} \quad [3]$$

Using the minimum "1" level at the line receiver input ($V_{ID} \geq +25\ mV = V_{ID}^{+}$), the equation becomes

$$I_{OH}(MIN) = I_1 - I_2 + I_{IH}(MAX) \quad [4]$$

and $I_{IH}(MAX) = 75\ \mu A$

$$I_{OH}(MIN) = \frac{V_{ID}^{+}}{R1} + \frac{V + V_{ID}^{+}}{R2} + 75\ \mu A \quad [5]$$

Solving these equations ([3] and [5]) simultaneously yields R1 and R2.

As an example, assume a memory system with 4 outputs wired-ORed to a sense amplifier, requiring a chip access time of 460 nsec. Then the associated current and resistor values are:

$I_{OLT}(MAX) = 152.3\ \mu A + 3\ (5\ \mu A) = 167.3\ \mu A$

$I_{OH}(MIN) = 511.12\ \mu A$

Therefore:

$R1 = 190\ \Omega$

$R2 = 16.5\ K\Omega$

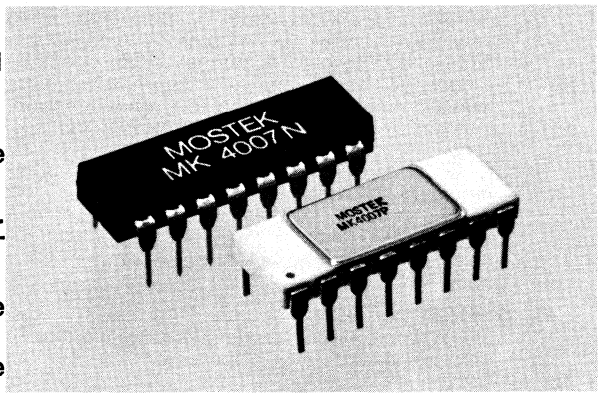
Sense amplifiers vary from the very fast, low-threshold types to the slower, high-threshold kind. The ideal choice will depend on the application. Fig. 1-A and the guidelines in this note are intended to help the designer tailor his sense amplifier design to meet the speed and cost requirements of his particular application.

It should also be noted that a portion of the output current from the memory chip is used to charge the capacitance on the data output. If the output impedance differs greatly from the specified load, this current must also be calculated.

MK 4007P
MK 4007N

256 BIT
MOS Random Access Memory

MOSTEK



FEATURES:

- ☐ Versatile RAM can replace any existing 1101-type 256x1 MOS RAM pin for pin.
- ☐ Ion-implanted for superior performance.
- ☐ **Lower power dissipation:** TOTAL 370 mW max over entire temperature range.
- ☐ **Faster access time:** Typically 525 ns with V_D and V_{DD} at −9V.
- ☐ **Less temperature-sensitive:** specified over entire AMBIENT temperature range 0° to 75°C.
- ☐ **Tight control of output sink current capabilities:** made possible by use of depletion-mode transistors.
- ☐ **No restrictions** on address input sequence, skew, or rise and fall times.
- ☐ Full DTL/TTL compatibility.
- ☐ Wide power supply range: +5V; −6.5 to −15V.

APPLICATIONS:

Ideal for small buffer storage requiring low cost, superior performance, and bipolar compatibility, such as:

- ☐ Scratchpad memories
- ☐ Data link buffers
- ☐ Key-to-tape buffers
- ☐ Tape-to-printer buffers
- ☐ Editing memories.

DESCRIPTION

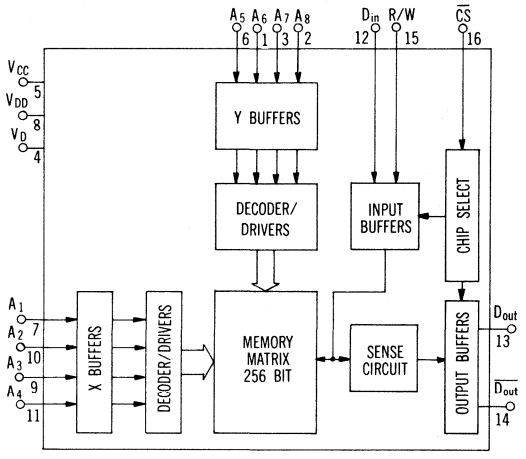
Ion-implantation processes used in manufacturing the Mostek MK 4007 P Random Access MOS Memory result in a low-cost device with performance exceeding other industry types over the entire temperature and voltage supply ranges. It may be used to replace any existing 1101 type RAM pin for pin.

The depletion-load ion-implantation technique allows the fabrication of both depletion and enhancement mode transistors on the same chip. The result is not only superior operating characteristics within the region usually specified for devices of this type, but also wider operational areas without severe performance degradation. For example, while specifications for this device are given for V_D and V_{DD} from −7 to −13.2V, V_D and V_{DD} may actually range from −6.5 to −15 V (see DC Operating Conditions and Fig. 1). Access times are improved (see Fig. 2); power dissipation is reduced (see Fig. 3) and output sink current capabilities are improved (see Fig. 4). The device is less temperature-dependent (see Figures 5 and 6) and is specified over the *entire* ambient temperature range of 0° to 75°C.

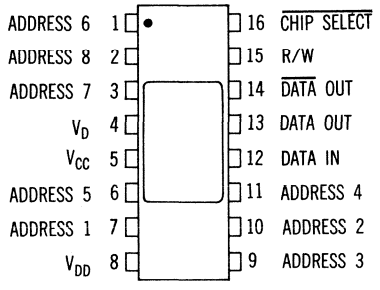
The ion-implantation process also makes the MK 4007 P RAM fully TTL/DTL compatible at all inputs and outputs.

The 4007 P is a static memory, requiring no clocks or refreshing. Data is written into the address location by applying a logic "1" to the R/W input. Addressing the desired location, with the chip enabled and R/W at logic "0", provides a non-destructive read-out (NDRO) of true and complement data. A "Chip Select" allows output buffers to be open-circuited during disable time for wire ORing. All inputs are protected against static charge accumulation.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Voltage on Any Terminal Relative to V_{CC} . . . . . + 0.3 V to −25 V
Operating Temperature Range (Ambient) . . . . . 0°C to +75°C
Storage Temperature Range (Ambient) . . . . . −55° to +150°C

DC OPERATING CONDITIONS

(Ambient Temperature Range: 0°C to +75°C)

		PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{CC}	Supply Voltage	4.75	5.0	5.25	V	
	V_{DD}	Supply Voltage	−6.5	−9.0	−15.0	V	See Fig. 1 for
	V_D	Supply Voltage	−6.5	−9.0	−15.0	V	V_D, V_{DD} differential
INPUTS	V_{IL}	Logic "0" Voltage, any input		0	+0.8	V	
	V_{IH}	Logic "1" Voltage, any input	V_{CC} −2.0	V_{CC}	V_{CC}+0.3	V	

ELECTRICAL CHARACTERISTICS

(Ambient Temperature Range: 0°C to +75°C. V_{CC} = +5 V ±5%;
$V_D = V_{DD}$ = −7 V to −13.2 V, unless otherwise specified.)

		PARAMETER	MIN	TYP(1)	MAX	UNITS	CONDITIONS
POWER	I_D	Supply Current. V_D		8.0	16	mA	$V_D = V_{DD}$ = −9V ± 5% Outputs open-circuited.
	I_{DD}	Supply Current, V_{DD}		4.0	9	mA	
	P_D	Power Dissipation, Total		170	370	mW	
	I_D	Supply Current. V_D			19	mA	$V_D = V_{DD}$ = −13.2 V V_{CC} = +5.25 V Outputs open-circuited.
	I_{DD}	Supply Current, V_{DD}			10	mA	
	P_D	Power Dissipation, Total			535	mW	
	P_{SDBY}	Power Dissipation, Standby		30	75	mW	$V_D = V_{CC}$; V_{DD} = −9V ±5%
INPUTS	$I_{I(L)}$	Input Leakage Current			1.0	μA	V_{IN} = 0 V, T_A = 25°C
	C_{IN}	Input Capacitance, Any Logic Input		7	10	pF	T_A = 25°C, F. meas. = 1 MHz; Tested input = V_{CC}
	$C_{V(D)}$	Capacitance, V_D Power Supply		35		pF	
OUTPUTS	I_{OL}	Output Current, Logic "0"	3.2	5.6		mA	V_O = +0.40 V
	I_{OH}	Output Current, Logic "1"	−1.0	−4.2		mA	V_O = +2.6 V
	I_{OLC}	Output Clamp Current, Logic "0"			8.0	mA	V_O = −1.0 V
	$I_{O(L)}$	Output Leakage Current			1.0	μA	$V_O = V_{CC}$ −5V; $\overline{CS}$ = Logic 1; T_A = 25°C.
	C_{OUT}	Output Capacitance		7	10	pF	T_A = 25°C; F meas. = 1 MHz; $V_O = V_{CC}$

NOTES:

(1) Typical values at V_{CC} = +5 V, $V_D = V_{DD}$ = −9.0 V*, T_A = 25°C.
(*Except Standby Power)

TIMING

(Ambient Temperature Range: 0°C to 75°C; V_{CC} = +5 V ±5%; $V_D = V_{DD}$ = −7V to −13.2 V, unless otherwise specified. See Notes 1 and 2.)

		PARAMETER	MIN	TYP	MAX	UNITS	
OPERATING CONDITIONS	t_{wc}	Write Cycle Time	700			ns	
	t_{wd}	Write Set-up Delay	300			ns	
	t_{wp}	Write Pulse Width	400			ns	
	t_{dld}	Data Lead Time	300			ns	
	t_{dlg}	Data Lag Time	0			ns	
	t_{cw}	Chip Select Pulse Width	400			ns	
DYNAMIC CHAR.	t_{ACC}	Access Time		525	900	ns	$V_D = V_{DD}$ = −9V ±5%.
	t_{RC}	Read Cycle Time			800	ns	(See Note 3.)
	t_{ACC}	Access Time			1.0	µs	$V_D = V_{DD}$ = −7V to −13.2V.
	t_{RC}	Read Cycle Time			900	ns	(See Note 3.)
	t_{OH}	Data Output Hold Time	100			ns	
	t_{CSE}	Chip-Select-to-Output Enable			300	ns	
	t_{CSD}	Chip-Select-to-Output Disable			300	ns	

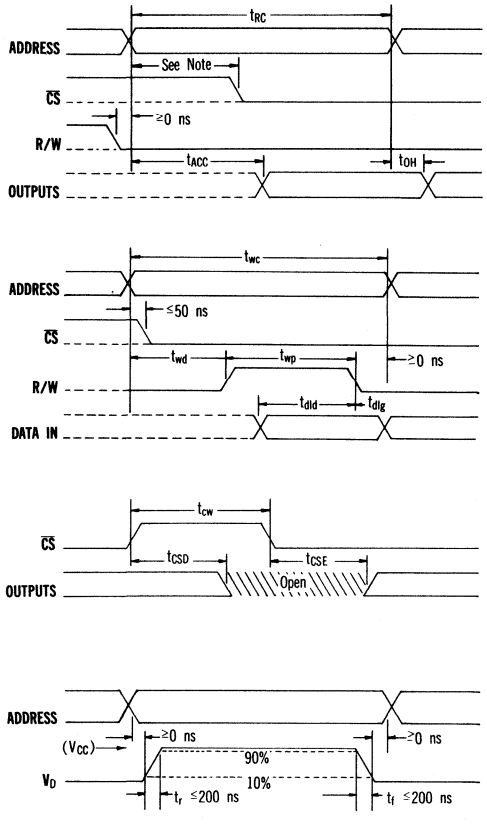
NOTES:

(1) All measurements to the 1.5 V level; inputs for test are 0 to 5 V and ≤10 ns rise and fall times; output is loaded with 1 TTL and approx. 20 pF.

(2) R/W should be brought to logical "0" whenever address bits are changed; however, there are no restrictions on rise and fall times of address bits, nor on the sequence (or skew) of address bit changes.

(3) Read Cycle may be "pipe-lined," i.e., the minimum hold time (t_{OH}) may be subtracted from the maximum access time (t_{ACC}).

TIMING



READ CYCLE

Reading is accomplished with R/W (Read/Write) and $\overline{CS}$ (Chip Select) at logical "0."

NOTE: $\overline{CS}$ logical "1" overlap time shown must be 300 ns (max t_{CSE}) less than the desired access time; e.g., if desired access time t_{ACC} = 1.2 µs, then $\overline{CS}$ should go to logical "0" no later than 900 ns following address change.

WRITE CYCLE

Writing is accomplished with R/W at logical "1" and $\overline{CS}$ at logical "0." $\overline{CS}$ at logical "1" may overlap the address change as much as 50 ns. R/W may be taken to logical "0" coincidentally with an address change, but should not overlap an address change while in the logical "1" state.

$\overline{\text{CHIP SELECT}}$

Chip Select at logical "1" causes the normal push-pull output buffers to be open-circuited for purposes of wire-ORing. The Chip Select may be used to access the memory at a faster rate by maintaining a constant address and selecting individual chips with the Chip Select input.

POWER SWITCHING

During standby operation the MK 4007 P will dissipate only 30 mW of power (typically) if the peripheral power supply, V_D, is reduced to V_{CC}. The R/W input may be maintained at logical "0" or "1"; however, if R/W is at logical "1," Chip Select should also be logical "1" (to disable chip during standby operation). With the return of power, either read or write cycles may commence as described above.

TYPICAL PERFORMANCE CURVES

FIG. 1: POWER SUPPLY OPERATING REGION & DIFFERENTIAL

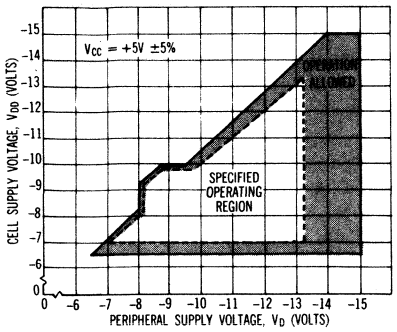


FIG. 2: ACCESS TIME VS SUPPLY VOLTAGE, (V_D)

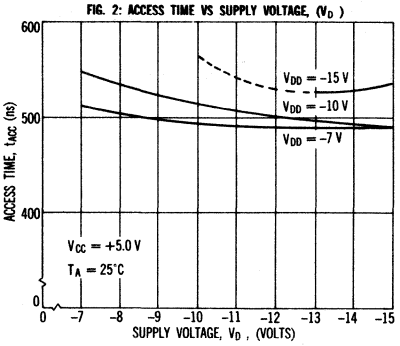


FIG. 3: TOTAL POWER DISSIPATION, (P_D), VS SUPPLY VOLTAGE, (V_D and V_{DD})

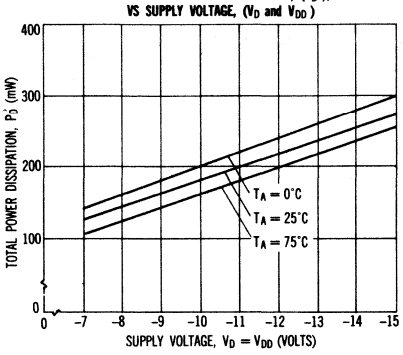


FIG. 4: OUTPUT CURRENT VS OUTPUT VOLTAGE

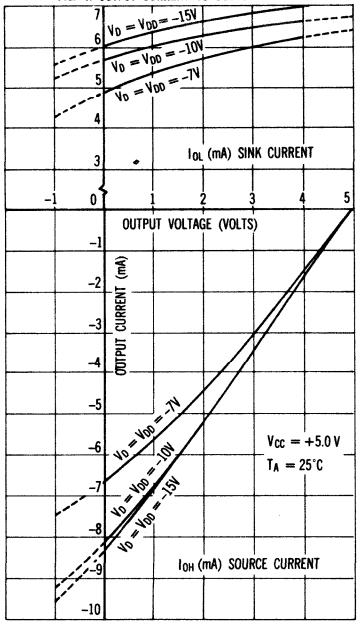


FIG. 5: OUTPUT CURRENT VS AMBIENT TEMPERATURE

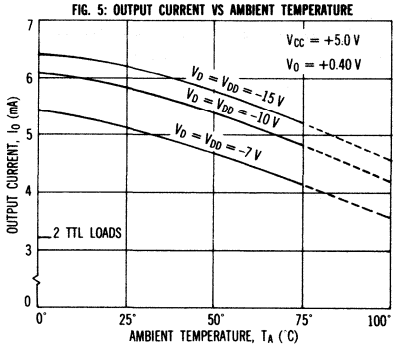


FIG. 6: WORST-CASE ACCESS TIME VS SUPPLY VOLTAGE (At Various Capacitances and Ambient Temperatures)

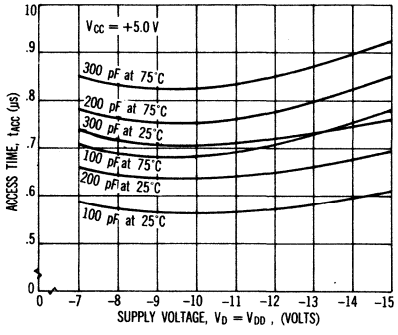


FIG. 7: SUPPLY CURRENT, (I_D and I_{DD}), VS SUPPLY VOLTAGE (V_D and V_{DD})

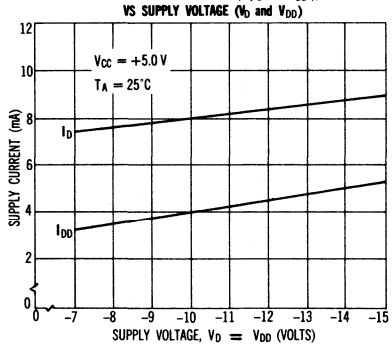
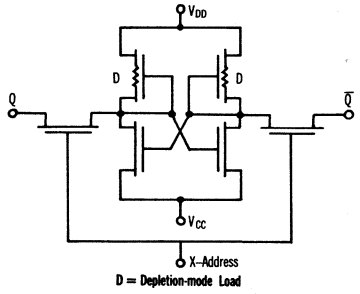
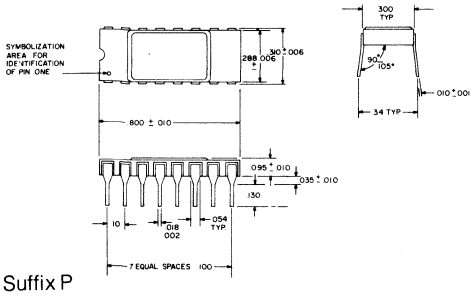


FIG. 8: MK 4007 P MEMORY CELL

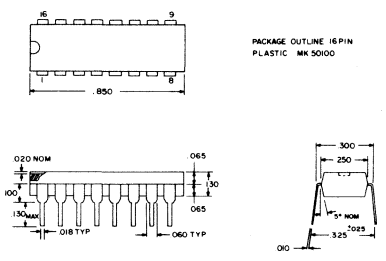


PACKAGE
16-pin ceramic dual-in-line



Suffix P

PACKAGE
16-pin plastic dual-in-line



Suffix N

SUPPLEMENT MK 4007P -4 MK 4007N -4

256-BIT
MOS Random Access Memory

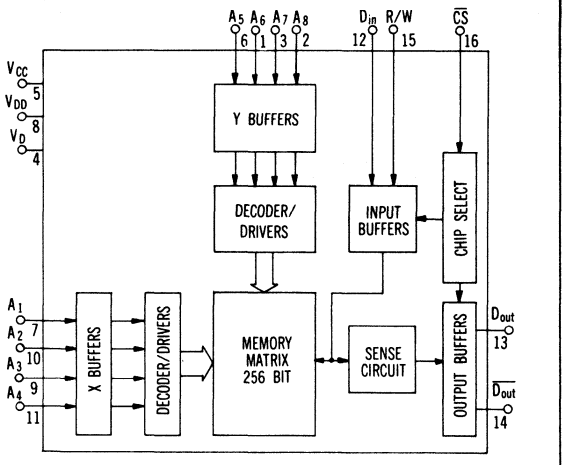
MOSTEK

- Low-cost 256x1 RAM in 16-pin package.
- Identical with Mostek's MK 4007 P in all specifications except output current

DESCRIPTION

This economical version of Mostek's 256x1 bit RAM is identical with the MK 4007 P in all electrical characteristics except output current. Performance, operating conditions, timing characteristics, package, and all other specifications are identical with the MK 4007 P. See the MK 4007 P Data Sheet for additional information.

FUNCTIONAL DIAGRAM



ELECTRICAL CHARACTERISTICS

(Ambient Temperature Range: 0°C to +75°C. V_{CC} = +5 V ±5%; V_D = V_{DD} = −7 V to −13.2 V, unless otherwise specified.)

		PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
POWER	I_D	Supply Current, V_D		8.0	16	mA	V_D = V_{DD} = −9 V ±5%
	I_{DD}	Supply Current, V_{DD}		4.0	9	mA	Outputs open-circuited.
	P_D	Power Dissipation, Total		170	370	mW	
	I_D	Supply Current, V_D			19	mA	V_D = V_{DD} = −13.2 V
	I_{DD}	Supply Current, V_{DD}			10	mA	V_{CC} = +5.25 V
	P_D	Power Dissipation, Total			535	mW	Outputs open-circuited.
	P_{SDBY}	Power Dissipation, Standby		30	75	mW	V_D = V_{CC}; V_{DD} = −9V ±5%
INPUTS	$I_{I(L)}$	Input Leakage Current			1.0	μA	V_{IN} = O V, T_A = 25°C
	C_{IN}	Input Capacitance, Any Logic Input		7	10	pF	T_A = 25°C, F. Meas. =
	$C_{V(D)}$	Capacitance, V_D Power Supply		35		pF	1 MHz; Tested input = V_{CC}
OUTPUTS	I_{OL}	Output Current, Logic "0": @ T_A = 25°C	3.0	5.6		mA	V_O = +0.40 V; V_{CC} = 5.0 V ±5%
		Output Current, Logic "0": @ T_A = 70°C	2.0			mA	V_O = +0.40 V; V_D = V_{DD} = −9.0 V
	I_{OH}	Output Current, Logic "1"	−1.0	−4.2		mA	V_O = +2.6 V; ±10%
	I_{OLC}	Output Clamp Current, Logic "0"			8.0	mA	V_O = −1.0 V
	$I_{O(L)}$	Output Leakage Current			1.0	μA	V_O = V_{CC} −5V; $\overline{CS}$ = Logic 1; T_A = 25°C.
	C_{OUT}	Output Capacitance		7	10	pF	T_A = 25°C; F meas. = 1 MHz; V_O = V_{CC}

NOTES:

(1) Typical values at V_{CC} = +5 V, V_D = V_{DD} = −9.0 V*, T_A = 25°C.
(*Except Standby Power)

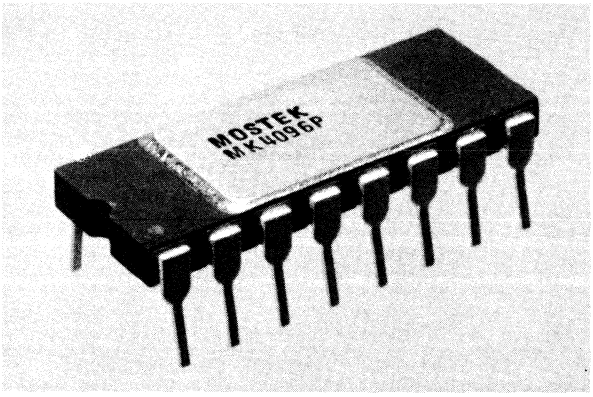
MK4096P-6
MK4096P-16

4096x 1 BIT DYNAMIC
MOS Random Access Memory

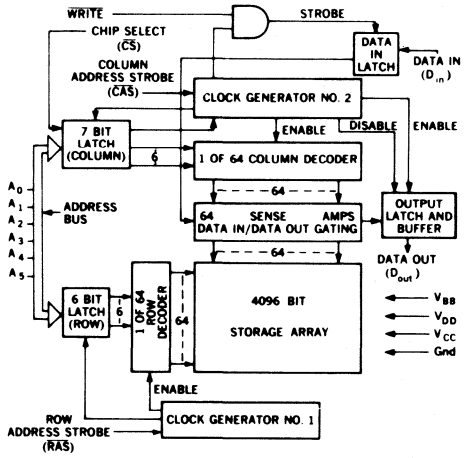
MOSTEK

FEATURES:

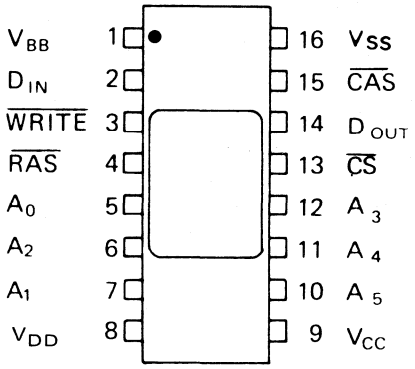
- ☐ Standard 16-pin DIP
- ☐ All inputs TTL compatible
- ☐ On-chip latches for addresses, chip select, and data in
- ☐ Three-state TTL compatible output
- ☐ Chip select decode does not add to access time
- ☐ Output data latched and valid into next cycle
- ☐ Read and write cycles of 375 nsec (-6) and 425 nsec (-16)
- ☐ Access times of 250 nsec (-6) and 300 nsec (-16)
- ☐ Low power: active power under 380 mW (-16) standby power under 24 mW



FUNCTIONAL DIAGRAM



PIN CONNECTIONS



DESCRIPTION:

The MK 4096 is a 4096x1 bit dynamic random access memory circuit fabricated with MOSTEK's special Self-Aligned, Poly-Interconnect, N-Channel (SPIN) process to minimize cell area and optimize circuit performance. The single transistor cell uses a dynamic storage technique and each of the 64 row addresses requires refreshing every 2 milliseconds.

A unique multiplexing and latching technique for the address inputs permits the MK 4096 to be packaged in a standard 16-pin DIP on 0.3 inch centers. This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

System oriented features on the MK 4096 include direct interfacing capability with TTL, 6 instead of 12 address lines to drive, on-chip registers which can eliminate the need for interface registers, input logic levels selected to optimize the noise immunity, and two chip select methods to allow the user to determine the speed/power characteristics of his memory system.

ADDRESSING:

The 12 address bits required to decode 1 of 4096 cell locations are multiplexed onto the 6 address pins and latched into the on-chip row and column address latches. The Row Address Strobe ($\overline{RAS}$) latches the 6 row address bits into the chip. The Column Address Strobe ($\overline{CAS}$) latches the 6 column address bits plus Chip Select ($\overline{CS}$) into the chip. Since the Chip Select signal is not required until well into the cycle, its decoding time does not add to the system access or cycle time.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} . . . . . −0.5V to +25.0V
Operating Temperature T_A (Ambient) . . . . . 0°C to 70°C
Storage Temperature (Ambient) . . . . . −55°C to 150°C

RECOMMENDED DC OPERATING CONDITIONS

($0° \leq T_A \leq 70°C$)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	11.4	12.0	12.6	volts	1
V_{CC}	Supply Voltage	V_{SS}	5.0	V_{DD}	volts	1, 6
V_{SS}	Supply Voltage	0	0	0	volts	1
V_{BB}	Supply Voltage	−4.5	−5.0	−5.5	volts	1
V_{IH}	Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$ $\overline{WRITE}$	2.4	5.0	7.0	volts	1, 8
V_{IL}	Logic 0 voltage, all inputs	−1.0	0	.8	volts	1, 8
V_{IHC}	Logic 1 Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.7	5.0	7.0	volts	1, 8

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{DD} = 12.0V ± 5%; V_{CC} = 5.0V ± 10%; V_{SS} = 0V, V_{BB} = −5.0V ± 10%)

	PART NUMBER	4096-6		4096-16			
	PARAMETER	MIN	MAX	MIN	MAX	UNITS	NOTES
I_{DD1}	Average V_{DD} Power Supply Current		35		30	mA	10
I_{CC}	V_{CC} Power Supply Current					mA	3
I_{BB}	Average V_{BB} Power Supply Current		75		75	µA	
I_{DD2}	Standby V_{DD} Power Supply Current		2		2	mA	
$I_{I(L)}$	Input Leakage Current (any input)		10		10	µA	4
$I_{O(L)}$	Output Leakage Current		10		10	µA	5
V_{OH}	Output Logic 1 Voltage @ I_{OUT} = −5 mA	2.4		2.4		volts	
V_{OL}	Output Logic 0 Voltage @ I_{OUT} = 2 mA		0.4		0.4	volts	

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS [14]

($0°C \leq T_A \leq 70°C$) (V_{DD} = 12.0V ± 5%; V_{CC} = 5.0V ± 10%, V_{SS} = 0V, V_{BB} = – 5.0V ± 10%)

	PART NUMBER	4096-6		4096-16			
	PARAMETER	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Random Read or Write Cycle Time	375		425		nsec	9, 12
t_{RAC}	Access Time from Row Address Strobe		250		300	nsec	9
t_{CAC}	Access Time from Column Address Strobe		140		165	nsec	11
t_{OFF}	Output Buffer Turn-Off Delay	0	65	0	80	nsec	
t_{RP}	Row Address Strobe Precharge Time	125		125		nsec	
t_{RCL}	Row to Column Strobe Lead Time	70	110	90	135	nsec	
t_{CPW}	Column Address Strobe Pulse Width	140		165		nsec	
t_{AS}	Address Set-Up Time	0		0		nsec	
t_{AH}	Address Hold Time	60		80		nsec	
t_{CH}	Chip Select Hold Time	100		100		nsec	
t_T	Rise And Fall Times	5	50	5	50	nsec	13
t_{RCS}	Read Command Set-Up Time	0		0		nsec	
t_{RCH}	Read Command Hold Time	0		0		nsec	
t_{WCH}	Write Command Hold Time	110		130		nsec	2
t_{WP}	Write Command Pulse Width	140		165		nsec	
t_{CRL}	Column To Row Strobe Lead Time	–40	+40	–50	+50	nsec	
t_{CWL}	Write Command to Column Strobe Lead Time	140		165		nsec	
t_{DS}	Data In Set-Up Time	0		0		nsec	7
t_{DH}	Data In Hold Time	110		130		nsec	7
t_{RFSH}	Refresh Period		2		2	msec	
t_{MOD}	Modify Time	0	10	0	10	µsec	

AC ELECTRICAL CHARACTERISTICS [14]

$(0°C \leq T_A \leq 70°C)$ $(V_{DD} = 12.0V \pm 5\%, V_{CC} = 5.0 \pm 10\%, V_{SS} = 0V, V_{BB} = -5.0V \pm 10\%)$

	PARAMETER	MIN	MAX	UNITS	NOTES
C_{I1}	Input Capacitance ($A_0 - A_5$)		10	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$ $\overline{CAS}$, D_{IN}, $\overline{WRITE}$, $\overline{CS}$)		7	pF	
C_O	Output Capacitance (D_{OUT})		8	pF	

NOTES:

1. All voltages referenced to V_{SS}.
2. Write Command Hold Time is important only when performing normal random write cycles. During read-write or read-modify-write cycles, the Write Command Pulse Width is the limiting parameter.
3. Depends upon output loading. The V_{CC} supply is connected to the output buffer only.
4. All device pins at 0 volts except V_{BB} at −5 volts and pin under test which is at +10 volts.
5. Output disabled by chip select input.
6. Output voltage will swing from V_{SS} to V_{CC} independent of differential between V_{SS} and V_{CC}.
7. These parameters are referenced to the $\overline{CAS}$ leading edge in random write cycle operation and to the $\overline{WRITE}$ leading edge in read-write or read-modify-write cycles.
8. Input voltages greater than TTL levels (0 to 5V) require device operation at reduced speed.
9. Assumes that $t_{RCL} + t_T \leq t_{RCL\ (max.)}$. If $t_{RCL} + t_T > t_{RCL\ (max.)}$, then t_{RC} and t_{RAC} will be longer by the amount $t_{RCL} + t_T$ exceeds $t_{RCL\ (max.)}$.
10. Current is proportional to speed with maximum current measured at fastest cycle rate.
11. Assumes $t_{RCL} + t_T \geq t_{RCL}$ (max). If not, the access time is controlled by t_{RAC}.
12. The minimum cycle time is achieved by compensating for $\overline{RAS}$ rise and fall times with t_{CRL}. The minimum cycle time is then constrained by t_{RCL} (max) + t_{CPW} + t_{RP}.
13. Rise and fall times measured between V_{IH} or V_{IHC} and V_{IL}.
14. Assumes t_T = 10 nsec.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$. The last of these signals making its negative transition is the strobe for the Data In register. This permits several options in the write timing. In a write cycle, if the $\overline{WRITE}$ input is brought low prior to $\overline{CAS}$, the Data In is strobed by $\overline{CAS}$ and the set-up and hold time are referenced to this signal. If the cycle is to be a read-write cycle, or read-modify-write cycle, then the $\overline{WRITE}$ input will not go to a logic 0 until after access time. But now, because $\overline{CAS}$ is already at a logic 0, the Data In is strobed in by $\overline{WRITE}$ and the set-up and hold time are referenced to it.

At the beginning of a memory cycle the state of the Data Out Latch and buffer depend on the previous memory cycle. If during the previous cycle the chip was unselected, the output buffer will be in its open-circuit condition. If the previous cycle was a read, read-write, or read-modify-write cycle and the chip was selected, then the output latch and buffer will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. If the previous cycle was a write cycle ($\overline{WRITE}$ active low before access time) and the chip was selected, then the output latch and buffer will contain a logic 1. Regardless of the state of the output it will remain valid until $\overline{CAS}$ goes negative. At that time the output will unconditionally go to its open-circuit state. It will remain open circuit until access time. At access time the output will assume the proper state for the type of cycle performed. If the chip is unselected, it will not accept a $\overline{WRITE}$ command and the output will remain in the open-circuit state.

INPUT/OUTPUT LEVELS

All inputs,including the two address strobes,will interface with TTL. The high impedance, low capacitance input characteristics simplify input driver selection by allowing use of standard logic elements rather than specially designed driver elements. Even though the inputs may be driven directly by TTL gates, pull-up or termination resistors are normally required in a system to prevent ringing of the input signals due to line inductance and reflections. In high speed memory systems, transmission line techniques must be employed on the signal lines to achieve optimum system speeds. Series rather than parallel terminations may be employed at some degradation of system speed.

The three-state output buffer is a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS}, for a logic 0. The resistance to V_{CC} is 500-ohms maximum and 150-ohms typically. The resistance to V_{SS} is 200-ohms maximum and 100-ohms typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may be unpowered without affecting the MK 4096P refresh operation. This allows all system logic except the $\overline{RAS}/\overline{CAS}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

REFRESH

Refresh of the cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses every 2 milliseconds or less. Any read cycle refreshes the selected row, regardless of the state of the Chip Select. A write, read-write, or read-modify-write cycle also refreshes the selected row but the chip should be unselected to prevent writing data into the selected cell.

POWER DISSIPATION/STANDBY MODE

Most of the circuitry used in the MK 4096P is dynamic and draws power only as the result of an address strobe edge. Because the power is not drawn during the whole time the strobe is active, the dynamic power is a function of operating frequency. Typically, the power is 120mW at a 1 μsec cycle time for the MK 4096P; with a worst case power of less than 380mW at a 425 nsec cycle time. To reduce the overall system power the Row Address Strobe ($\overline{RAS}$) must be decoded and supplied to only the selected chips. The $\overline{CAS}$ must be supplied to all chips (to turn off the unselected outputs). But those chips that did not receive a $\overline{RAS}$ will not dissipate any power on the $\overline{CAS}$ edges, except for that required to turn off the output. If the $\overline{RAS}$ is decoded and supplied to the selected chips, then the Chip Select input of all chips can be at a logic 0. The chips that receive a $\overline{CAS}$ but no $\overline{RAS}$ will be unselected (output open-circuited) regardless of the Chip Select input.

The current waveforms for the current drawn from the V_{DD} and V_{BB} supplies are shown in Figure A. Since the current is pulsed, proper power distribution and bypassing techniques are required to maintain system power supply noise levels at an acceptable level. Low inductance supply lines for V_{DD} and V_{SS} are desirable. A minimum of one 0.01 microfarad, low inductance, bypass capacitance per two MK 4096P devices and one 6.8 microfarad electrolytic capacitor per eight MK 4096P devices on each of the V_{DD} and V_{BB} supply lines is desirable. A noise level of less than 0.5 volts peak-to-peak on both V_{DD} and V_{BB} should be a design goal.

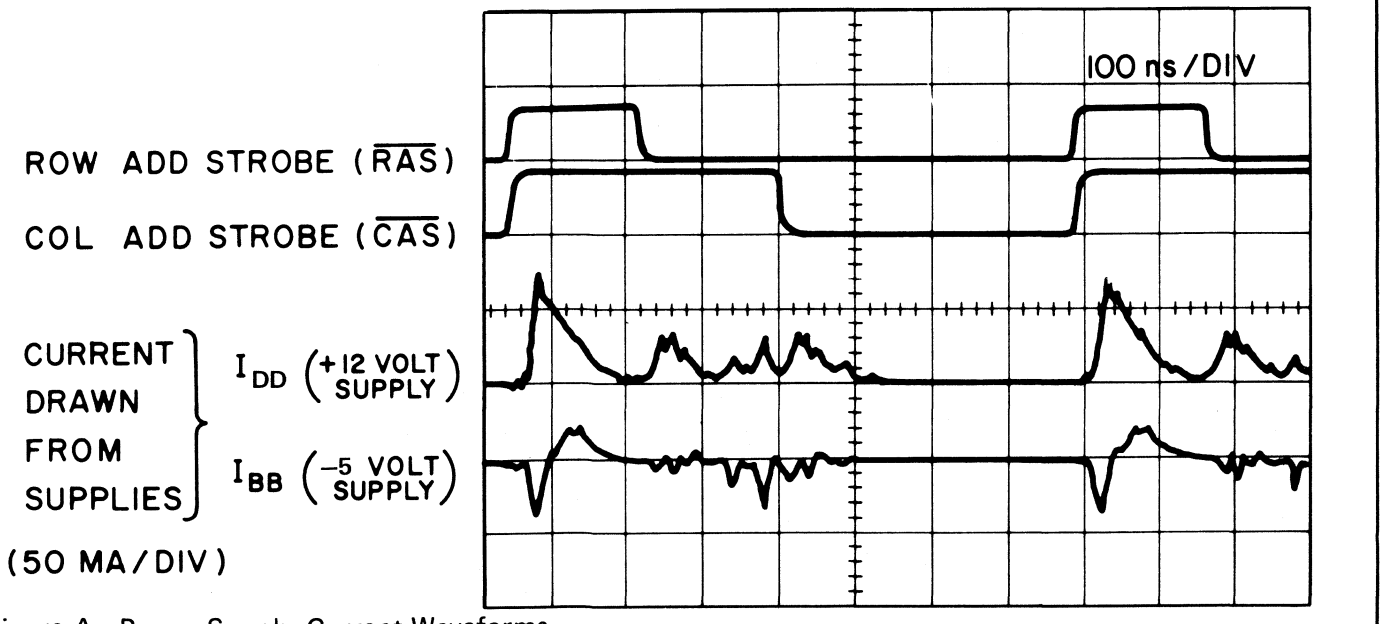
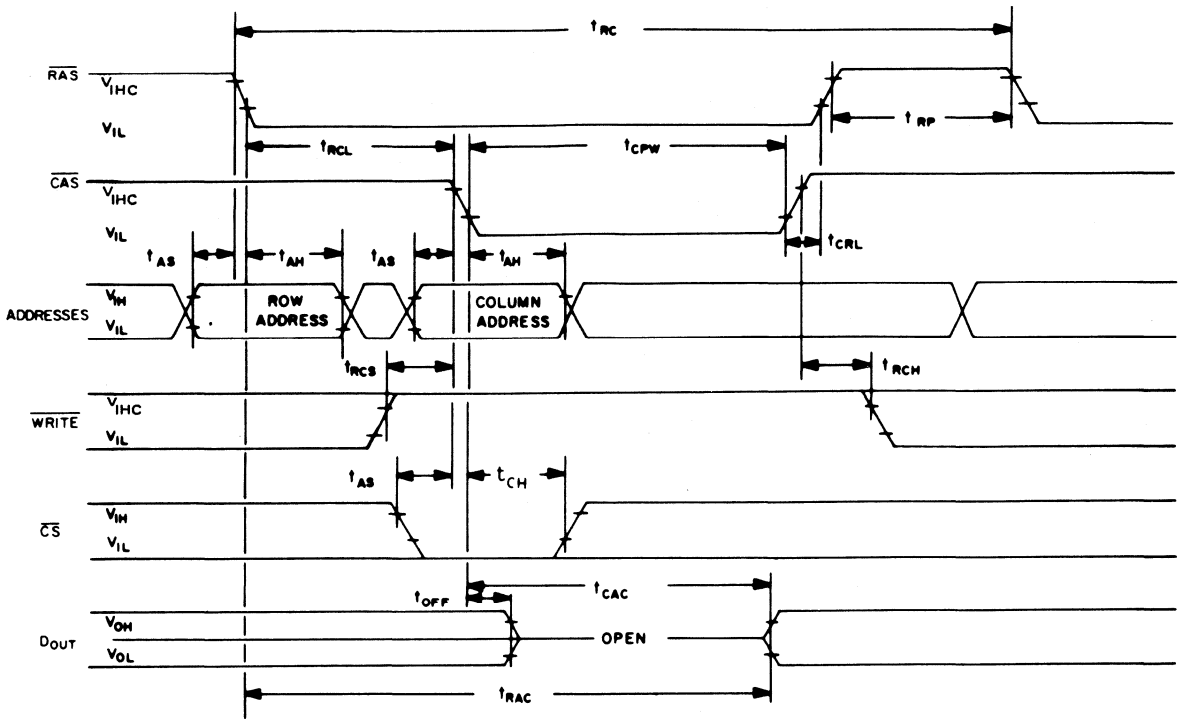
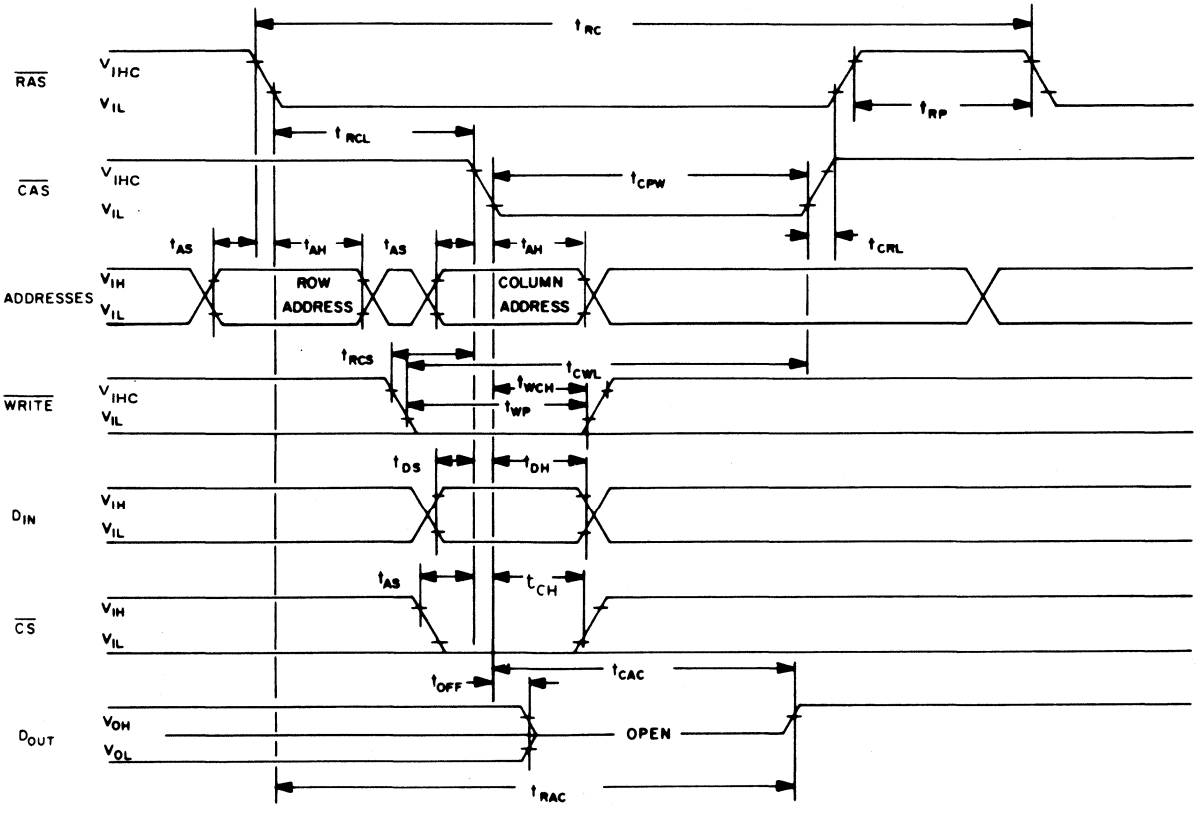


Figure A. Power Supply Current Waveforms

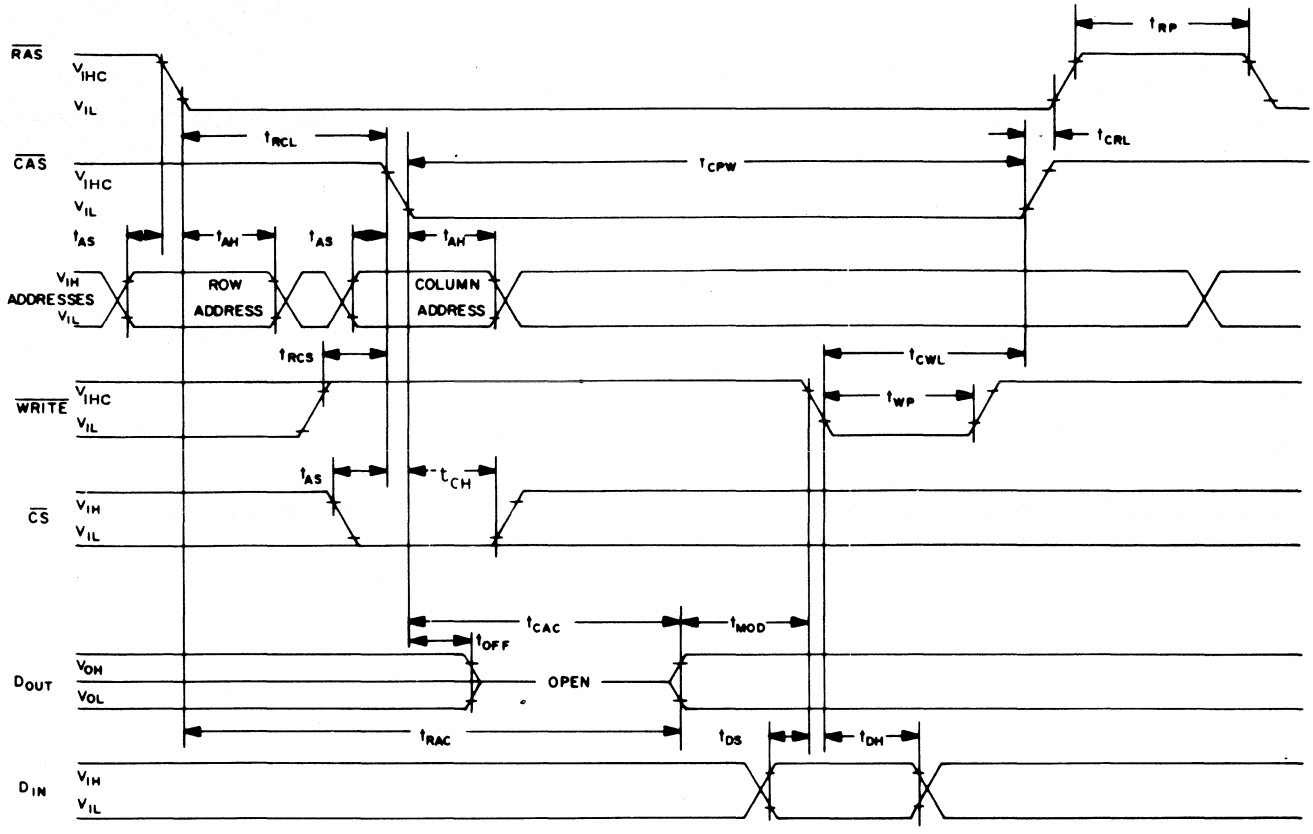
READ CYCLE



WRITE CYCLE

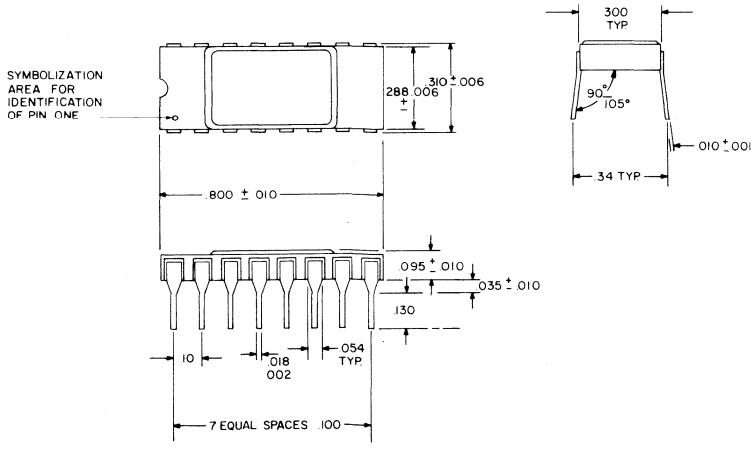


READ-MODIFY-WRITE CYCLE



PACKAGE DESCRIPTION

16-lead side-brazed ceramic dual-in-line hermetic package



SUPPLEMENT MK4096P-11

4096x 1 **BIT DYNAMIC**

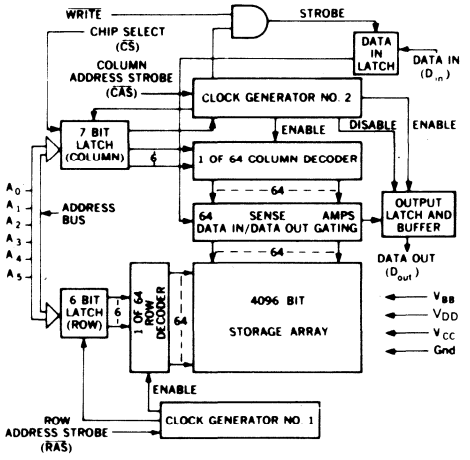
MOS Random Access Memory

MOSTEK

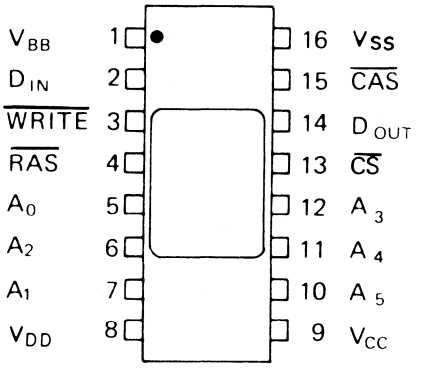
FEATURES:

- ☐ Standard 16-pin DIP
- ☐ All inputs TTL compatible
- ☐ On-chip latches for addresses, chip select, and data in
- ☐ Three-state TTL compatible output
- ☐ Chip Select decode does not add to access time
- ☐ Output data latched and valid into next cycle
- ☐ Read and write cycles of 500 nsec
- ☐ Access time of 350 nsec
- ☐ Low power: active power under 380 mW
  standby power under 24 mW

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



DESCRIPTION:

The MK 4096 is a 4096x1 bit dynamic random access memory circuit fabricated with MOSTEK's special Self-Aligned, Poly-Interconnect, N-Channel (SPIN) process to minimize cell area and optimize circuit performance. The single transistor cell uses a dynamic storage technique and each of the 64 row addresses requires refreshing every 2 milliseconds.

A unique multiplexing and latching technique for the address inputs permits the MK 4096 to be packaged in a standard 16-pin DIP on 0.3 inch centers. This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

System oriented features on the MK 4096 include direct interfacing capability with TTL, 6 instead of 12 address lines to drive, on-chip registers which can eliminate the need for interface registers, input logic levels selected to optimize the noise immunity, and two chip select methods to allow the user to determine the speed/power characteristics of his memory system.

ADDRESSING:

The 12 address bits required to decode 1 of 4096 cell locations are multiplexed onto the 6 address pins and latched into the on-chip row and column address latches. The Row Address Strobe ($\overline{RAS}$) latches the 6 row address bits into the chip. The Column Address Strobe ($\overline{CAS}$) latches the 6 column address bits plus Chip Select ($\overline{CS}$) into the chip. Since the Chip Select signal is not required unitl well into the cycle, its decoding time does not add to the system access or cycle time.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} ..... −0.5V to +25.0V
Operating Temperature T_A (Ambient) ..... 0°C to 70°C
Storage Temperature (Ambient) ..... −55°C to 150°C

RECOMMENDED DC OPERATING CONDITIONS
$(0° \leq T_A \leq 70° C)$

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	11.4	12.0	12.6	volts	1
V_{CC}	Supply Voltage	V_{SS}	5.0	V_{DD}	volts	1, 6
V_{SS}	Supply Voltage	0	0	0	volts	1
V_{BB}	Supply Voltage	−4.5	−5.0	−5.5	volts	1
V_{IH}	Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4	5.0	7.0	volts	1, 8
V_{IL}	Logic 0 voltage, all inputs	−1.0	0	.8	volts	1, 8
V_{IHC}	Logic 1 Voltage $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.7	5.0	7.0	volts	1, 8

DC ELECTRICAL CHARACTERISTICS
$(0° C \leq T_A \leq 70° C)$ $(V_{DD} = 12.0V \pm 5\%; V_{CC} = 5.0V \pm 10\%; V_{SS} = 0V, V_{BB} = -5.0V \pm 10\%)$

	PARAMETER	MIN	MAX	UNITS	NOTES
I_{DD1}	Average V_{DD} Power Supply Current		30	mA	10
I_{CC}	V_{CC} Power Supply Current			mA	3
I_{BB}	Average V_{BB} Power Supply Current		75	μA	
I_{DD2}	Standby V_{DD} Power Supply Current		2	mA	
$I_{I(L)}$	Input Leakage Current (any input)		10	μA	4
$I_{O(L)}$	Output Leakage Current		10	μA	5
V_{OH}	Output Logic 1 Voltage@ $I_{OUT} = -5mA$	2.4		volts	
V_{OL}	Output Logic 0 Voltage@ $I_{OUT} = -2mA$		0.4	volts	

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS [14]

($0°C \leq T_A \leq 70°C$) ($V_{DD} = 12.0V \pm 5\%$; $V_{CC} = 5.0V \pm 10\%$, $V_{SS} = 0V$, $V_{BB} = -5.0V \pm 10\%$)

	PARAMETER	MIN	MAX	UNITS	NOTES
t_{RC}	Random Read or Write Cycle Time	500		nsec	9, 12
t_{RAC}	Access Time from Row Address Strobe		350	nsec	9
t_{CAC}	Access Time from Column Address Strobe		200	nsec	11
t_{OFF}	Output Buffer Turn-Off Delay	0	100	nsec	
t_{RP}	Row Address Strobe Precharge Time	150		nsec	
t_{RCL}	Row to Column Strobe Lead Time	110	150	nsec	
t_{CPW}	Column Address Strobe Pulse Width	200		nsec	
t_{AS}	Address Set-Up Time	0		nsec	
t_{AH}	Address Hold Time	100		nsec	
t_{CH}	Chip Select Hold Time	100		nsec	
t_T	Rise and Fall Times	5	50	nsec	13
t_{RCS}	Read Command Set-Up Time	0		nsec	
t_{RCH}	Read Command Hold Time	0		nsec	
t_{WCH}	Write Command Hold Time	150		nsec	2
t_{WP}	Write Command Pulse Width	200		nsec	
t_{CRL}	Column to Row Strobe Lead Time	–50	+50	nsec	
t_{CWL}	Write Command to Column Strobe Lead Time	200		nsec	
t_{DS}	Data In Set-Up Time	0		nsec	7
t_{DH}	Data In Hold Time	150		nsec	7
t_{RFSH}	Refresh Period		2	msec	
t_{MOD}	Modify Time	0	10	μsec	

AC ELECTRICAL CHARACTERISTICS [14]

($0°C \leq T_A \leq 70°C$) (V_{DD} = 12.0V ± 5%, V_{CC} = 5.0 ± 10%, V_{SS} = 0V, V_{BB} = −5.0V ± 10%)

	PARAMETER	MIN	MAX	UNITS	NOTES
C_{I1}	Input Capacitance ($A_0 - A_5$)		10	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, D_{IN}, $\overline{WRITE}$, $\overline{CS}$)		7	pF	
C_{IO}	Output Capacitance (D_{OUT})		8	pF	

NOTES:

1. All voltages referenced to V_{SS}.
2. Write Command Hold Time is important only when performing normal random write cycles. During read-write or read-modify-write cycles, the Write Command Pulse Width is the limiting parameter.
3. Depends upon output loading. The V_{CC} supply is connected to the output buffer only.
4. All device pins at 0 volts except V_{BB} at −5 volts and pin under test which is at +10 volts.
5. Output disabled by chip select input.
6. Output voltage will swing from V_{SS} to V_{CC} independent of differential between V_{SS} and V_{CC}.
7. These parameters are referenced to the $\overline{CAS}$ leading edge in random write cycle operation and to the $\overline{WRITE}$ leading edge in read-write or read-modify-write cycles.
8. Input voltages greater than TTL levels (0 to 5V) require device operation at reduced speed.
9. Assumes that $t_{RCL} + t_T \leq t_{RCL}$ (max.). If $t_{RCL} + t_T > t_{RCL}$ (max), then t_{RC} and t_{RAC} will be longer by the amount $t_{RCL} + t_T$ exceeds t_{RCL} (max).
10. Current is proportional to speed with maximum current measured at fastest cycle rate.
11. Assumes $t_{RCL} + t_T \geq t_{RCL}$ (max). If not, the access time is controlled by t_{RAC}.
12. The minimum cycle time is achieved by compensating for $\overline{RAS}$ rise and fall times with t_{CRL}. The minimum cycle time is then constrained by t_{RCL} (max) + t_{CPW} + t_{RP}.
13. Rise and fall times measured between V_{IH} or V_{IHC} and V_{IL}.
14. Assumes t_T = 10 nsec.

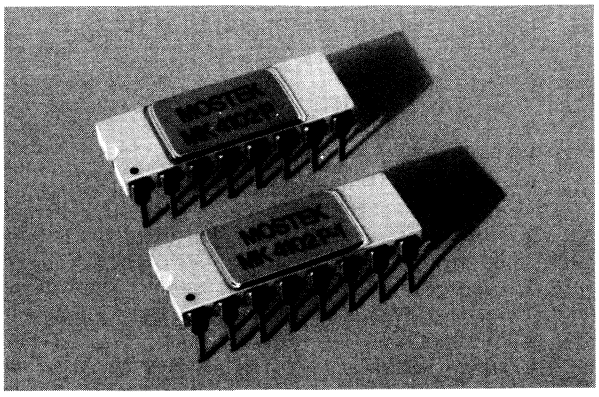
MK 4102 P
MK 4102 P-1

1024x 1 BIT STATIC
MOS Random Access Memory

MOSTEK

FEATURES

- ☐ Direct TTL compatibility — all inputs and output
- ☐ Three-State Output
- ☐ Single supply: +5V
- ☐ Fast access and cycle time:
  MK 4102P 1 μs; MK 4102P-1 450 ns
- ☐ Standard 16-pin DIP
- ☐ Completely static: no clocks or refreshing required



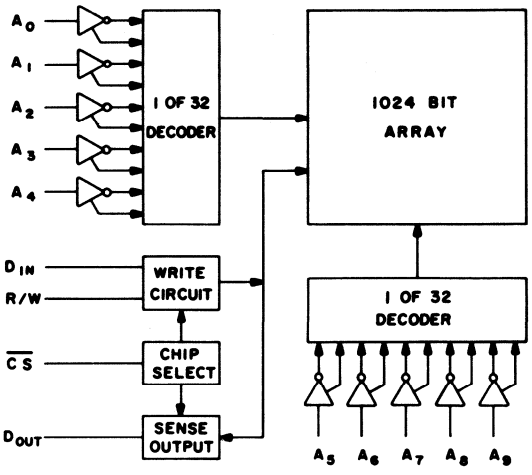
DESCRIPTION

The MOSTEK MK 4102 is a completely static 1024x1 bit random access memory circuit. It is constructed with N-channel silicon gate depletion mode technology.

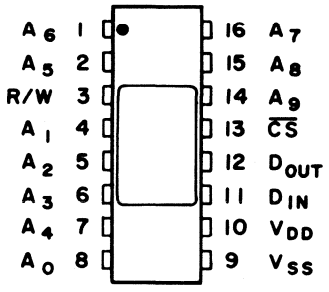
All inputs are directly compatible with TTL circuitry. The output of the memory is a three-state buffer. The high impedance "OFF" state coupled with the Chip Select ($\overline{CS}$) input permits the construction of large memory arrays with a minimum of additional circuitry. The static operation requires very little system overhead and makes the MK 4102 ideally suited to small and medium size memory applications.

The pin connections and functional operation are similar to MOSTEK's popular 1024x1 bit dynamic random access memory chips, the MK 4006 and the MK 4008. By eliminating the dynamic storage the refreshing is not required. This point, in conjunction with the direct TTL compatibility in and out of the memory chip, makes memory system design with the MK 4102 less complicated.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} ..... −0.5V to 7V
Operating Temperature (Ambient) ..... 0°C to 70°C
Storage Temperature (Ambient) ..... −55°C to +150°C

RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

	PARAMETER	MK 4102 P — MK 4102 P-1 MIN	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	4.75	5.25	volts	
V_{SS}	Supply Voltage	0	0	volts	
V_{IH}	Input Voltage, Logic 1	2.2	5.25	volts	
V_{IL}	Input Voltage, Logic 0	0	.65	volts	

RECOMMENDED AC OPERATING CONDITIONS[1] ($0°C \leq T_A \leq 70°C$)

	PARAMETER	MK 4102 P-1 MIN	MAX	MK 4102 P MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle	450		1000		nsec	
t_{WC}	Write Cycle	450		1000		nsec	
t_{WP}	Write Pulse Width	300		750		nsec	
t_{AW}	Address to Write Pulse Delay	100		200		nsec	
t_{DS}	Data Set-Up Time	330		800		nsec	
t_{DH}	Data Hold Time	50		100		nsec	
t_{CW}	Chip Select Pulse Width	200		300		nsec	
t_{ACW}	Address To Chip Select Delay		50		50	nsec	Write Cycle
t_{ACR}	Address To Chip Select Delay		250		700	nsec	Read Cycle
t_{WA}	Write Pulse to Address Delay	50		50		nsec	

DC ELECTRICAL CHARACTERISTICS ($V_{DD} = +5V \pm 5\%$, $V_{SS} = OV$, $0°C \leq T_A \leq 70°C$)

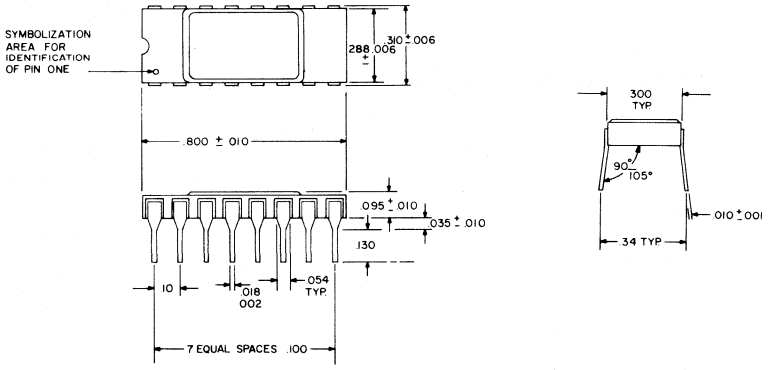
	PARAMETER	MK 4102 P — MK 4102 P-1 MIN	MAX	UNITS	NOTES
I_{DD}	Supply Current		70	mA	output open
I_{LI}	Input Leakage Current		10	μA	$V_{IN} = OV$ to 5.25V[2]
I_{LO}	Output Leakage Current		10	μA	$V_O = 0.4V$ to 5.25V[3]
V_{OH}	Output Voltage, Logic 1	2.2		volts	$I_{OH} = -100\mu A$
V_{OL}	Output Voltage, Logic 0		.40	volts	$I_{OL} = +3.2mA$

AC ELECTRICAL CHARACTERISTICS[1] ($V_{DD} = +5V \pm 5\%$, $V_{SS} = OV$, $0°C \leq T_A \leq 70°C$)

	PARAMETER	MK 4102 P-1 MIN	MAX	MK 4102 P MIN	MAX	UNITS	NOTES
t_{ACC}	Access Time		450		1000	nsec	
t_{CS}	Chip Select Time		200		300	nsec	
t_{CD}	Chip Deselect Time		200		300	nsec	
C_I	Input Capacitance (Any Input)		6		6	pF	f = 1MHz V_I = OV@25°C
C_O	Output Capacitance		10		10	pF	f = 1MHz V_I = OV@25°C

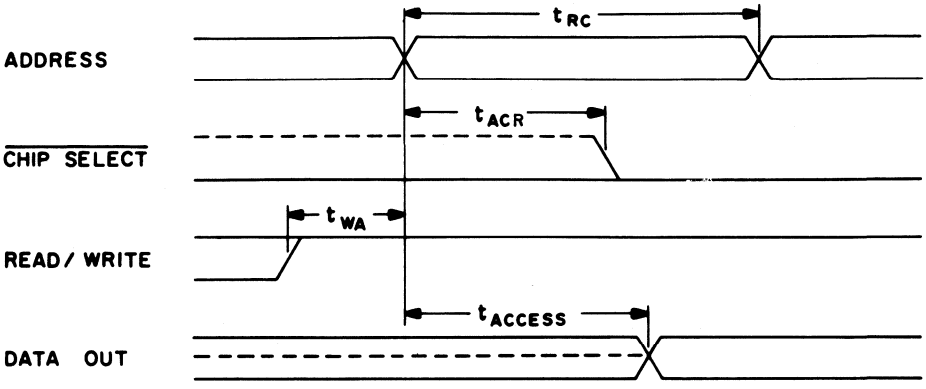
Notes: (1) AC Test Conditions: input voltage swings = +.4V to 2.4V, input rise and fall times = 20 nsec; measurement point on signals = 1.5V; and output load = 1 standard TTL load +100pF.
(2) $V_{SS} = V_{DD} = OV$
(3) Chip disabled

PACKAGE (16-lead ceramic dual-in-line hermetic package)

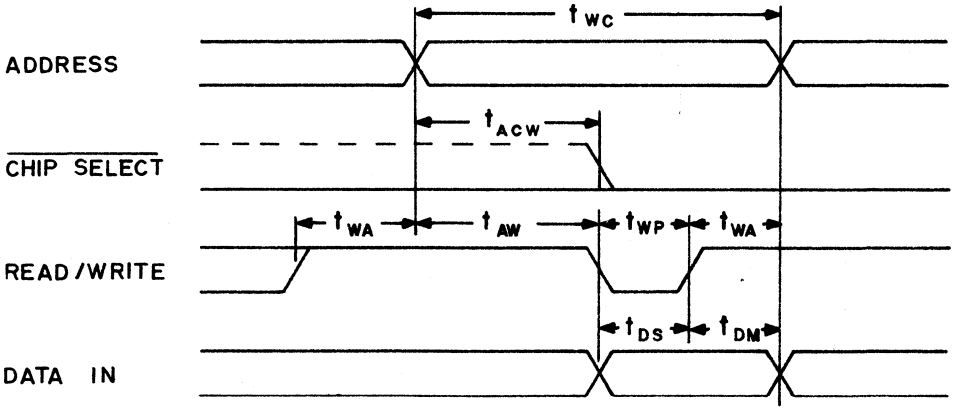


TIMING

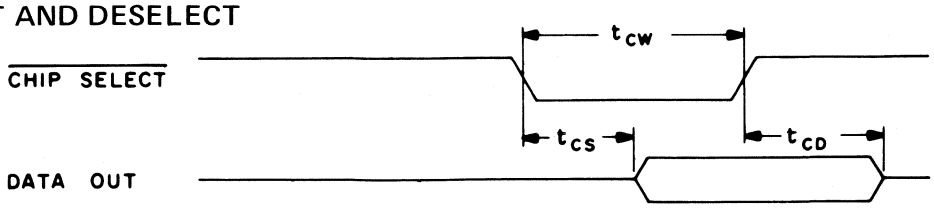
READ CYCLE



WRITE CYCLE



CHIP SELECT AND DESELECT



This timing assumes that the addresses for at least t_{ACR} prior to $\overline{\text{Chip Select}}$.

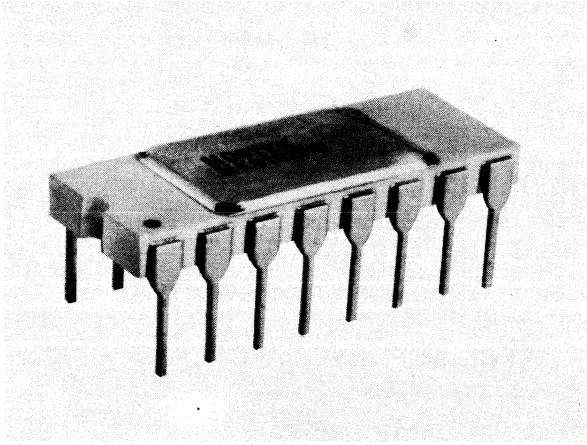
1024x1 BIT STATIC

MOS Random Access Memory

MOSTEK

FEATURES:

- ☐ Direct TTL compatibility – all inputs and output
- ☐ Three-State Output
- ☐ Single supply: +5V
- ☐ Fast access and cycle time: 275 ns
- ☐ Standard 16-pin DIP
- ☐ Completely static: no clocks or refreshing required



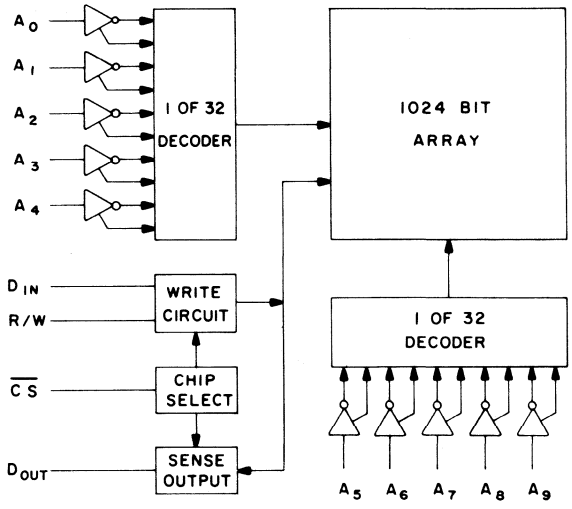
DESCRIPTION:

The MOSTEK MK 4102-6 is a completely static 1024x1 bit random access memory circuit. It is constructed with N-channel silicon gate depletion mode technology.

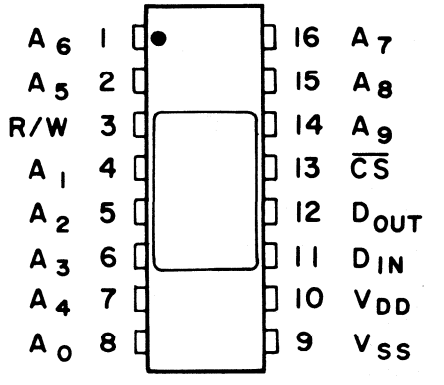
All inputs are directly compatible with TTL circuitry. The output of the memory is a three-state buffer. The high impedance "OFF" state coupled with the Chip Select (CS) input permits the construction of large memory arrays with a minimum of additional circuitry. The static operation requires very little system overhead and makes the MK 4102-6 ideally suited to small and medium size memory applications.

The pin connections and functional operation are similar to MOSTEK's popular 1024x1 bit dynamic random access memory chips, the MK 4006 and the MK 4008. By eliminating the dynamic storage the refreshing is not required. This point, in conjunction with the direct TTL compatibility in and out of the memory chip, makes memory system design with the MK 4102-6 less complicated.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} ..... –0.5V to 7V

Operating Temperature (Ambient) ..... 0°C to 70°C

Storage Temperature (Ambient) ..... –55°C to +150°C

RECOMMENDED DC OPERATING CONDITIONS ($0°C < T_A < 70°C$)

	PARAMETER	MIN	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	4.75	5.25	volts	
V_{SS}	Supply Voltage	0	0	volts	
V_{IH}	Input Voltage, Logic 1	2.2	5.25	volts	
V_{IL}	Input Voltage, Logic 0	0	.65	volts	

RECOMMENDED AC OPERATING CONDITIONS ($0°C < T_A < 70°C$)

	PARAMETER	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle	275		nsec	
t_{WC}	Write Cycle	275		nsec	
t_{WP}	Write Pulse Width	200		nsec	
t_{AW}	Address to Write Pulse Delay	0		nsec	
t_{DS}	Data Set-Up Time	175		nsec	
t_{DH}	Data Hold Time	50		nsec	
t_{CW}	Chip Select Pulse Width	175		nsec	
t_{WA}	Write Pulse To Address Delay	50	50	nsec	Write Cycle
t_{ACR}	Address to Chip Select Delay		125	nsec	Read Cycle
t_{OH}	Output Hold Time	50		nsec	Chip Must Remain Selected
t_{ACW}	Address to Chip Select Delay		50	nsec	Write Cycle

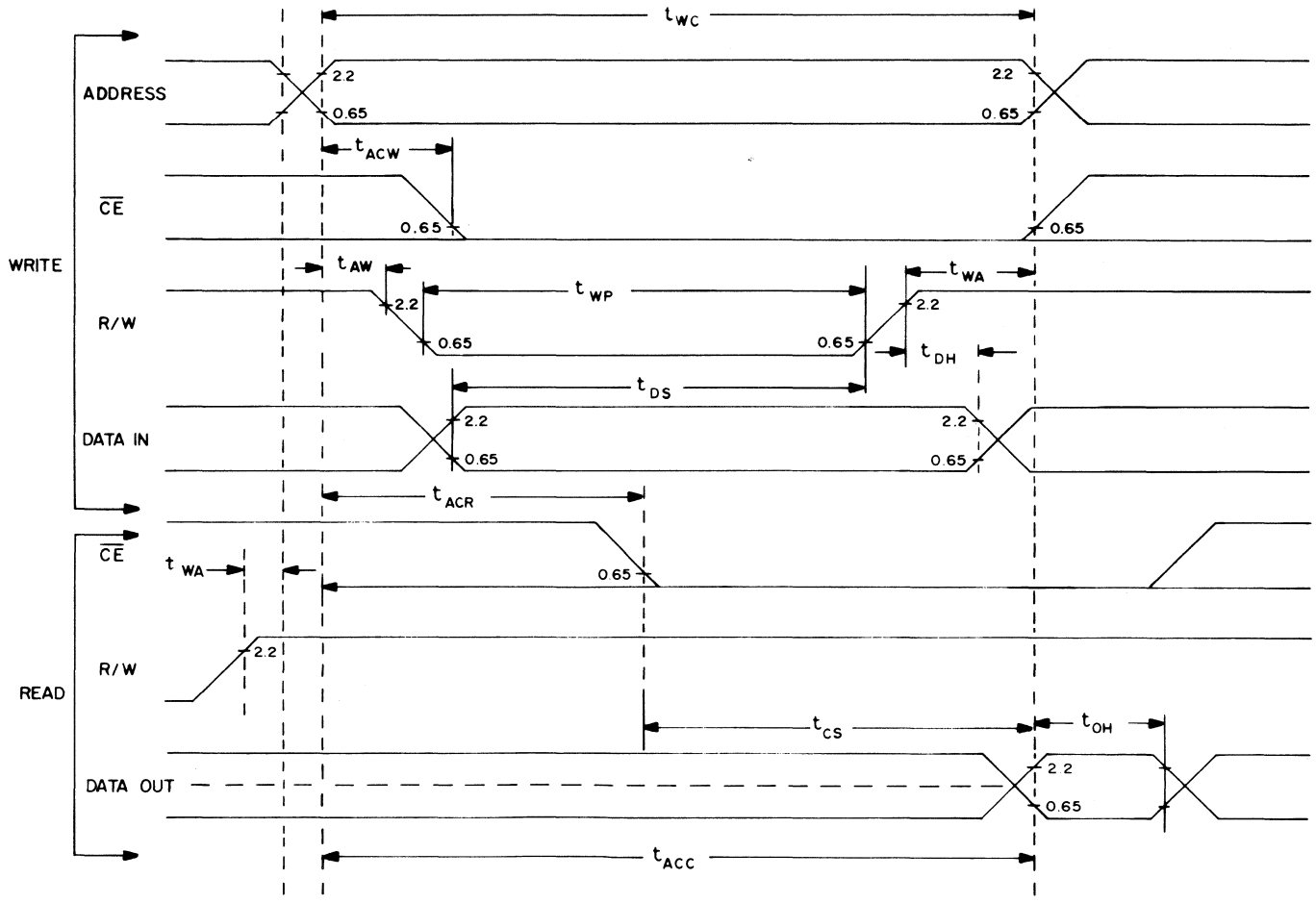
DC ELECTRICAL CHARACTERISTICS (V_{DD} = +5V ± 5%, V_{SS} = 0V, $0°C < T_A < 70°C$)

	PARAMETER	MIN	MAX	UNITS	NOTES
I_{DD}	Supply Current		80	mA	output open
I_{LI}	Input Leakage Current		10	µA	V_{IN} = 0V to 5.25 V
I_{LO}	Output Leakage Current		10	µA	V_O = 0.4V to 5.25V
V_{OH}	Output Voltage, Logic 1	2.2		volts	I_{OH} = -100 µA
V_{OL}	Output Voltage, Logic 0		.40	volts	I_{OL} = +3.2 mA

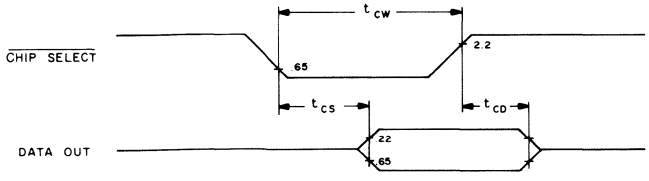
AC ELECTRICAL CHARACTERISTICS (V_{DD}= +5V ± 5%, V_{SS} = 0V, 0°C < T_A < 70°C)

	PARAMETER	MIN	MAX	UNITS	NOTES
t_{ACC}	Access Time		275	nsec	
t_{CS}	Chip Select Time		150	nsec	Address stable for T_{ARC}
t_{CD}	Chip Deselect Time		100	nsec	
C_I	Input Capacitance (Any Input)		5	pF	f = 1MHz V_I = 0V@25°C
C_O	Output Capacitance		10	pF	f = 1MHz V_I = 0V@25°C

TIMING

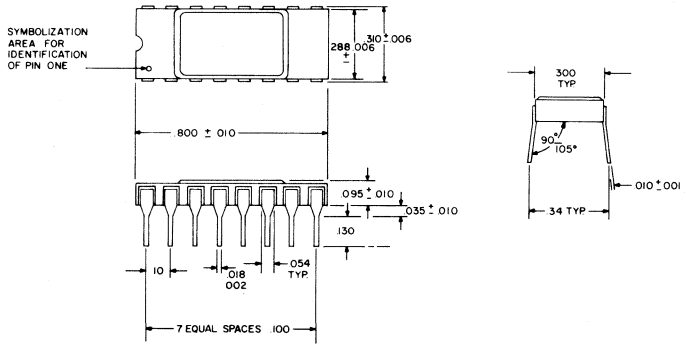


CHIP SELECT AND DESELECT



This timing assumes that the addresses for at least t_{ACR} prior to Chip Select.

PACKAGE (16-lead ceramic dual-in-line hermetic package)



PRELIMINARY

MK4200P-11

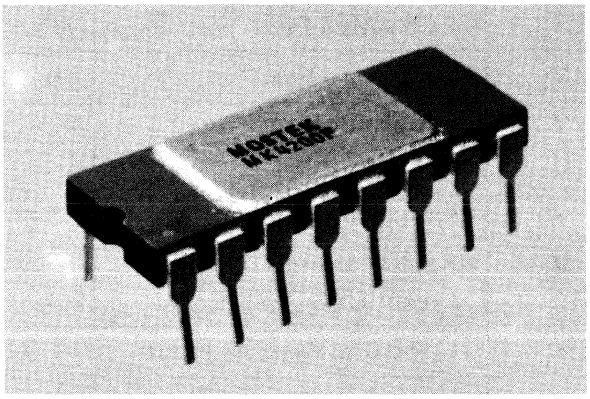
4096 x 1 **BIT DYNAMIC**

MOS Random Access Memory

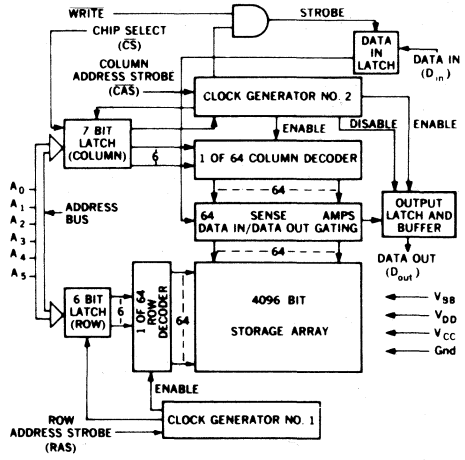
MOSTEK

FEATURES:

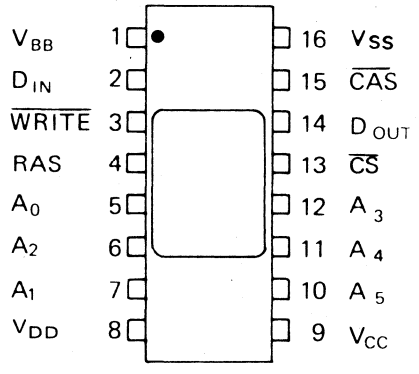
- ☐ Standard 16-pin DIP
- ☐ Inputs protected against static charge
- ☐ All inputs TTL compatible, except RAS
- ☐ On-chip latches for addresses, chip select, and data in
- ☐ Three-state TTL compatible output
- ☐ Chip select decode does not add to access time
- ☐ Output data latched and valid into next cycle
- ☐ Read and write cycles of 500 nsec
- ☐ Access times of 350 nsec
- ☐ Low power: active power under 300 mW
  standby power under .6mW
- ☐ No power-up sequence required



FUNCTIONAL DIAGRAM



PIN CONNECTIONS



DESCRIPTION:

The MK 4200 is a 4096 x 1 bit dynamic random access memory circuit fabricated with MOSTEK's special Self-Alligned, Poly-Interconnect. N-Channel (SPIN) process to minimize cell area and optimize circuit performance. The single transistor cell uses a dynamic storage technique and each of the 64 row addresses requires refreshing every 2 milliseconds.

A unique multiplexing and latching technique for the address inputs permits the MK 4200 to be packaged in a standard 16-pin DIP on 0.3 each centers. This package size provides high system bit densities and is compatable with widely available automated testing and insertion equipment.

System oriented features on the MK 4200 include very low standby power dissipation, direct interfacing capability with TTL, 6 instead of 12 address lines to drive, on-chip registers which can eliminate the need for interface registers, input logic levels selected to optimize the noise immunity, and two chip select methods to allow the user to determine the speed/power characteristics of his memory system.

ADDRESSING:

The 12 address bits required to decode 1 of 4096 cell locations are multiplexed onto the 6 address pins and latched into the on-chip row and column address latches. The Row Address Strobe (RAS) latches the 6 row address bits into the chip. The Column Address Strobe (CAS) latches the 6 column address bits plus Chip Select (CS) into the chip. Since the Chip Select signal is not required until well into the cycle, its decoding time does not add to the system access or cycle time.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} . . . . . -0.5V to +25.0V
Operating Temperature (Ambient) . . . . . 0° C to 70 °C
Storage Temperature (Ambient) . . . . . –55 °C to 150°C

RECOMMENDED DC OPERATING CONDITIONS

($0° \leq T_A \leq 70°$ C)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	11.4	12.0	12.6	volts	1
V_{CC}	Supply Voltage	V_{SS}	5.0	V_{DD}	volts	1,6
V_{SS}	Supply Voltage	0	0	0	volts	1
V_{BB}	Supply Voltage	–4.5	–5.0	–5.5	volts	1
V_{IH}	Logic 1 Voltage all inputs except $\overline{CAS}$, $\overline{WRITE}$	2.4	5.0	7.0	volts	1,8
V_{IL}	Logic 0 voltage, all inputs	–1.0	0	.8	volts	1,8
V_{IHC}	Logic 1 Voltage $\overline{CAS}$ $\overline{WRITE}$	2.7	5.0	7.0	volts	1,8
V_{IHR}	Logic 1 Voltage, RAS input	V_{DD}– 1	12.0	V_{DD}+ 1	volts	1
V_{ILR}	Logic 0 Voltage, RAS input	–1.0	0.0	+0.6	volts	1

DC ELECTRICAL CHARACTERISTICS

($0 °C \leq T_A \leq 70 °C$) (V_{DD}=12.0V±5%; V_{CC}=5.0V ±10%; V_{SS}= 0.V, V_{BB} = –5.0V ±10%)

	PARAMETER	MIN	MAX	UNITS	NOTES
I_{DDI}	Average V_{DD} Power Supply Current		25	mA	10
I_{CC}	V_{CC} Power Supply Current			mA	3
I_{BB}	Average V_{BB} Power Supply Current		75	μA	
I_{DD2}	Standby V_{DD} Power Supply Current		50	μA	5
$I_{I(L)}$	Input Leakage Current (any input)		10	μA	4
$I_{O(L)}$	Output Leakage Current		10	μA	5
V_{OH}	Output Logic 1 Voltage @ I_{out} = –5 mA	2.4		volts	
V_{OL}	Output Logic 0 Voltage @ Iout - 2 mA		0.4	volts	

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS [14]

(0 °C ≤ T_A ≤ 70 ° C) (V_{DD} = 12.0V ± 5%; V_{CC} =5.0V ± 10%, V_{SS} = OV, V_{BB} = –5.0V ± 10%)

	PARAMETER	MIN	MAX	UNITS	NOTES
t_{RC}	Random Read or Write Cycle Time	500		nsec	9, 12, 16
t_{RAC}	Access Time from Row Address Strobe		350	nsec	9
t_{CAC}	Access Time from Column Address Strobe		200	nsec	11
t_{OFF}	Output Buffer Turn-Off Delay	0	100	nsec	
t_{RP}	Row Address Strobe Precharge Time	150		nsec	
t_{RCL}	Row to Column Strobe Lead Time	110	150	nsec	11,15
t_{CPW}	Column Address Strobe Pulse Width	200		nsec	
t_{AS}	Address Set-Up Time	0		nsec	
t_{AH}	Address Hold Time	100		nsec	
t_{CH}	Chip Select Hold Time	100		nsec	
t_T	Rise And Fall Times	5	50	nsec	13
t_{RCS}	Read Command Set-Up Time	0		nsec	
t_{RCH}	Read-Command Hold Time	0		nsec	
t_{WCH}	Write Command Hold Time	150		nsec	2
t_{WP}	Write Command Pulse Width	150		nsec	
t_{CRL}	Column To Row Strobe Lead Time	–50	+50	nsec	
t_{CWL}	Write Command to Column Strobe Lead Time	200		nsec	7
t_{DS}	Data In Set-Up Time	0		nsec	7
t_{DH}	Data In Hold Time	150		nsec	7
t_{RFSH}	Refresh Period		2	msec	
t_{MOD}	Modify Time	0	10	μsec	

AC ELECTRICAL CHARACTERISTICS [14]

$(0\,^{\circ}C \leq T_A \leq 70\,^{\circ}C)$ $(V_{DD} = 12.0V \pm 5\%, V_{CC} = 5.0 \pm 10\%, V_{SS} = 0V, V_{BB} = -5.0V \pm 10\%)$

	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input Capacitance ($A_0 - A_5$)	6	10	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$ $\overline{CAS}$, D_{IN}, $\overline{WRITE}$, $\overline{CS}$)	4	7	pF	
C_0	Output Capacitance (D_{OUT})	5	8	pF	

NOTES

1. All voltages referenced to V_{SS} .
2. Write Command Hold Time is important only when performing normal random write cycles. During read-write or read modify-write cycles, the Write Command Pulse Width is the limiting parameter.
3. Depends upon output loading. The V_{CC} supply is connected to the output buffer only.
4. All device pins at 0 volts except V_{BB} at -5 volts and pin under test which is at +10 volts.
5. Output disabled by chip select input.
6. Output voltage will swing from V_{SS} to V_{CC} if $V_{CC} \leq V_{DD} - 4$ volts. If $V_{CC} > V_{DD} - 4$ volts. output will swing from V_{SS} to approx. $V_{DD} - 4$ volts.
7. These parameters are referenced to the $\overline{CAS}$ leading edge in random write cycle operation and to the $\overline{WRITE}$ leading edge in read-write or read-modify-write cycles.
8. Input voltages greater than TTL levels (0 to 5V) require device operation at reduced speed.
9. Assumes that $t_{RCL} + t_T \leq t_{RCL\,(max.)}$. If $t_{RCL\,(max.)}$ then t_{RC} and t_{RAC} will be longer by the amount $t_{RCL} + t_T$ exceeds $t_{RCL\,(max.)}$.
10. Current is proportional to speed with maximum current measured at fastest cycle rate.
11. Assumes $t_{RCL} + t_T \geq t_{RCL\,(max)}$. If not, the access time is controlled by t_{RAC}.
12. Minimum cycle time is limited by the rise and fall times of the RAS input.
13. Rise and fall time measured between V_{IH} and V_{IL} .
14. Assumes $t_T = 10$ nsec.
15. Max. limit is specified to achieve min. access time
16. Does not account for t_T .

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$. The last of these signals making its negative transition is the strobe for the Data In register. This permits several options in the write timing. In a write cycle, if the $\overline{WRITE}$ inputs are brought low prior to $\overline{CAS}$, the Data In is strobed by $\overline{CAS}$ and the set-up and hold time are referenced to this signal. If the cycle is to be a read-write cycle, or read-modify-write cycle, then the $\overline{WRITE}$ input will not go to a logic 0 until after access time. But now, because $\overline{CAS}$ is already at a logic 0, the Data In is strobed in by $\overline{WRITE}$ and the set-up and hold time are referenced to it.

At the beginning of a memory cycle the state of the Data Out Latch and buffer depend on the previous memory cycle. If during the previous cycle the chip was unselected, the output buffer will be in its open-circuit condition. If the previous cycle was a read, read-write, or read-modify-write cycle and the chip was selected, then the output latch and buffer will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. If the previous cycle was a write cycle ($\overline{WRITE}$ active low before access time) and the chip was selected, then the output latch and buffer will contain a logic 1. Regardless of the state of the output it will remain valid until $\overline{CAS}$ goes negative. At that time the output will unconditionally go to its open-circuit state. It will remain open circuit until access time. At access time the output will assume the proper state for the type of cycle performed. If the chip is unselected, it will not accept a $\overline{WRITE}$ command and the output will remain in the open-circuit state.

INPUT/ OUTPUT LEVELS

All inputs to the MK 4200 (except RAS) will interface with TTL. The high impedance, low capacitance input characteristics simplify input driver selection by allowing use of standard logic elements rather than specially designed driver elements. Even though the inputs may be driven directly by TTL gates, pull-up or termination resistors are normally required in a system to prevent ringing of the input signals due to line inductance and reflections. In high speed memory systems, transmission line techniques must be employed on the signal lines to achieve optimum system speeds. Series rather than parallel terminations may be employed at some degradation of system speed.

The RAS input has been specially designed so that very little steady state (D.C.) power is dissipated by the MK 4200 while in standby operation. In doing this, the RAS input requires a high level signal to activate the chip. The ROW ADDRESS STROBE input driver must be able to charge the capacitance load of the RAS input from within 0.6 volt of V_{SS} (0V) to within 1 volt of V_{DD} (+12V) in 50 nanoseconds.

The three-state output buffer is a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS}, for a logic 0. The resistance to V_{CC} is 500-ohms maximum and 150-ohms, typically. The resistance to V_{SS} is 200-ohms maximum and 100-ohms typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation the V_{CC} pin may be unpowered without affecting the MK 4096P refresh operation. This allows all system logic except the RAS/$\overline{\text{CAS}}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

REFRESH

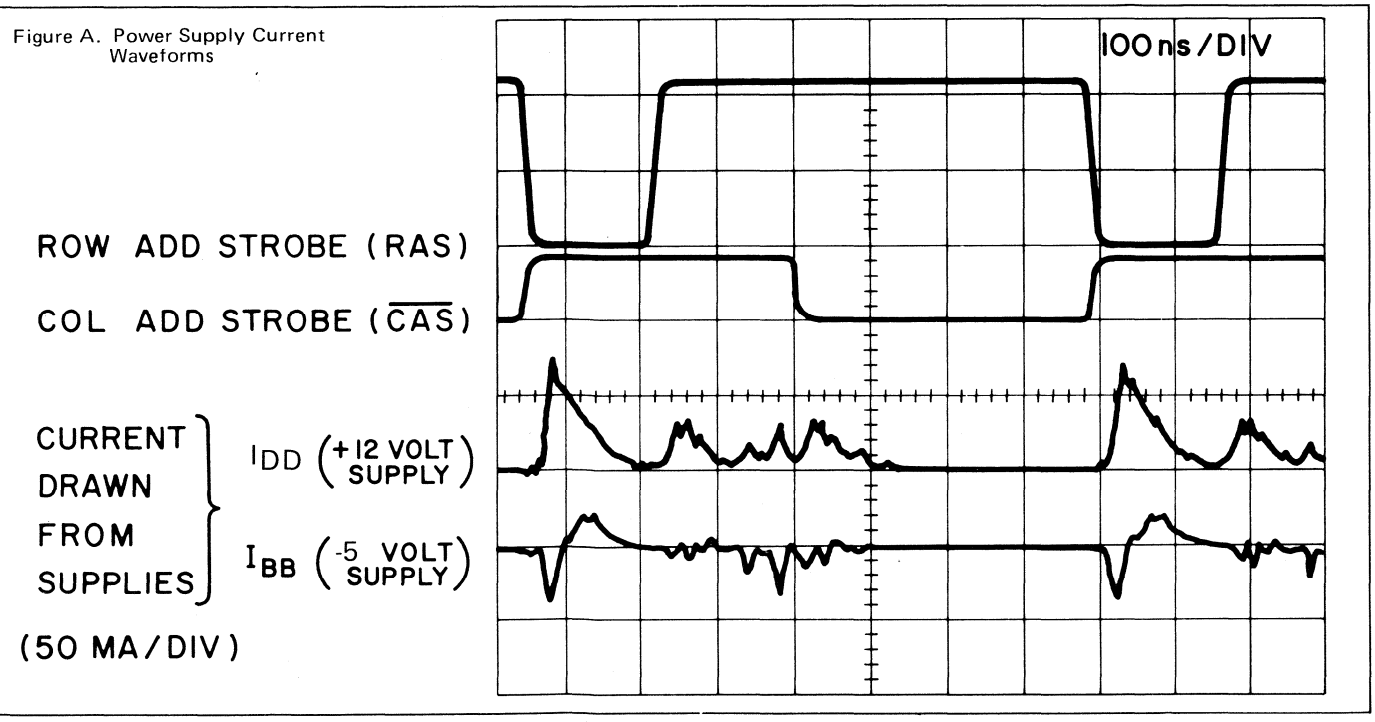
Refresh of the cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses every 2 milliseconds or less. Any read cycle refreshes the selected row, regardless of the state of the Chip Select. A write, read-write, or read-modify-write cycle also refreshes the selected row, but the chip should be unselected to prevent writing data into the selected cell.

POWER DISSIPATION/STANDBY MODE

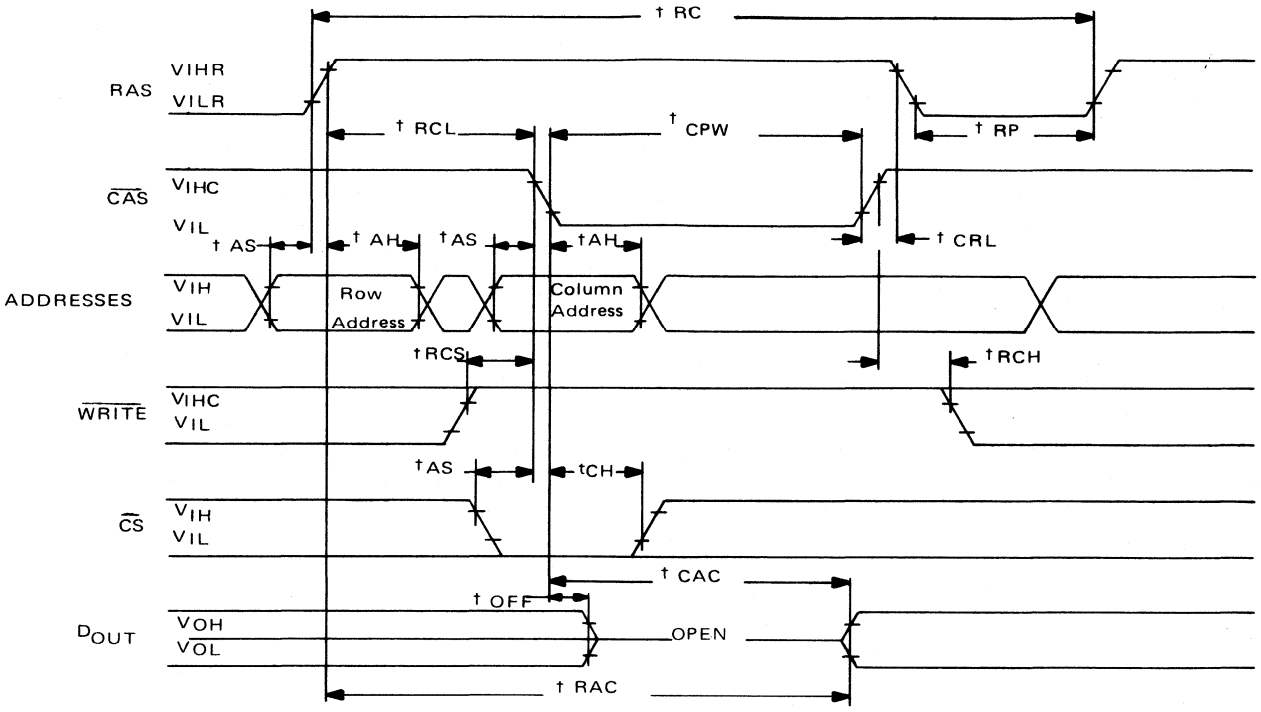
Most of the circuitry used in the MK 4200 is dynamic and draws power only as the result of an address strobe edge. Because the power is not drawn during the whole time the strobe is active, the dynamic power is a function of operating frequency. The power is 120mW at a 1μsec cycle time for the MK 4200P with a worst case power of less than 320 mW at a 500 nsec cycle time. To reduce the overall system power the Row Address Strobe (RAS) must be decoded and supplied to only the selected chips. The $\overline{\text{CAS}}$ must be supplied to all chips (to turn off the unselected out-puts). But those chips that did not receive a RAS will not dissipate any power on the $\overline{\text{CAS}}$ edges, except for that required to turn off the output. If the RAS is decoded and supplied to the selected chips, then the Chip Select input of all chips can be at a logic 0. The chips that receive a $\overline{\text{CAS}}$ but no RAS will be unselected (output open-circuited) regardless of the Chip Select input.

The current waveforms for the current drawn from the V_{DD} and V_{BB} supplies are shown in Figure A. Since the current is pulsed, proper power distribution and bypassing techniques are required to maintain system power supply noise levels at an acceptable level. Low inducatance supply lines for V_{DD} and V_{SS} are desirable. A minimum of one 0.01 microfarad, low inductance, bypass capacitance per two MK 4200P devices and one 6.8 microfarad electrolytic capacitor per eight MK 4200P devices on each of the V_{DD} and V_{BB} supply lines is desirable.

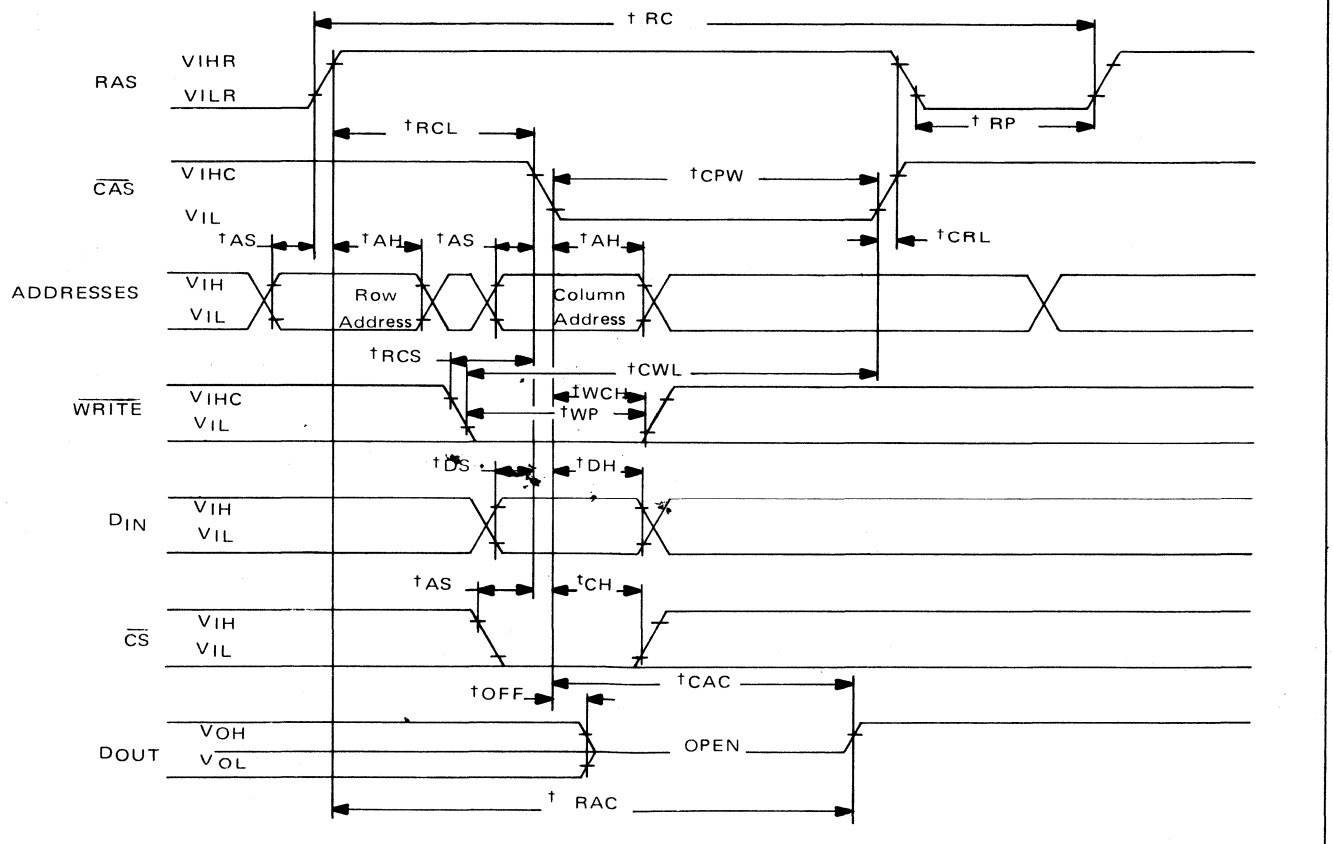
Figure A. Power Supply Current Waveforms



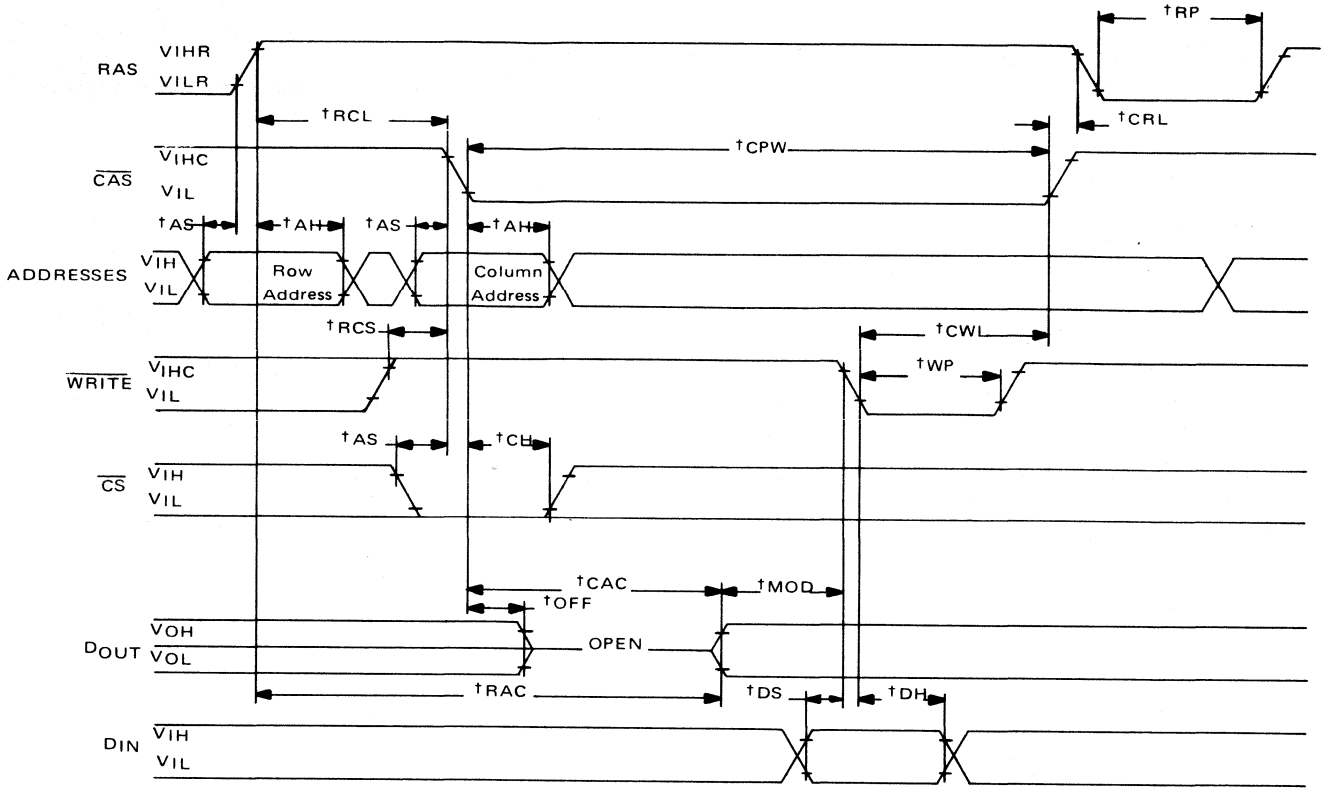
READ CYCLE



WRITE CYCLE

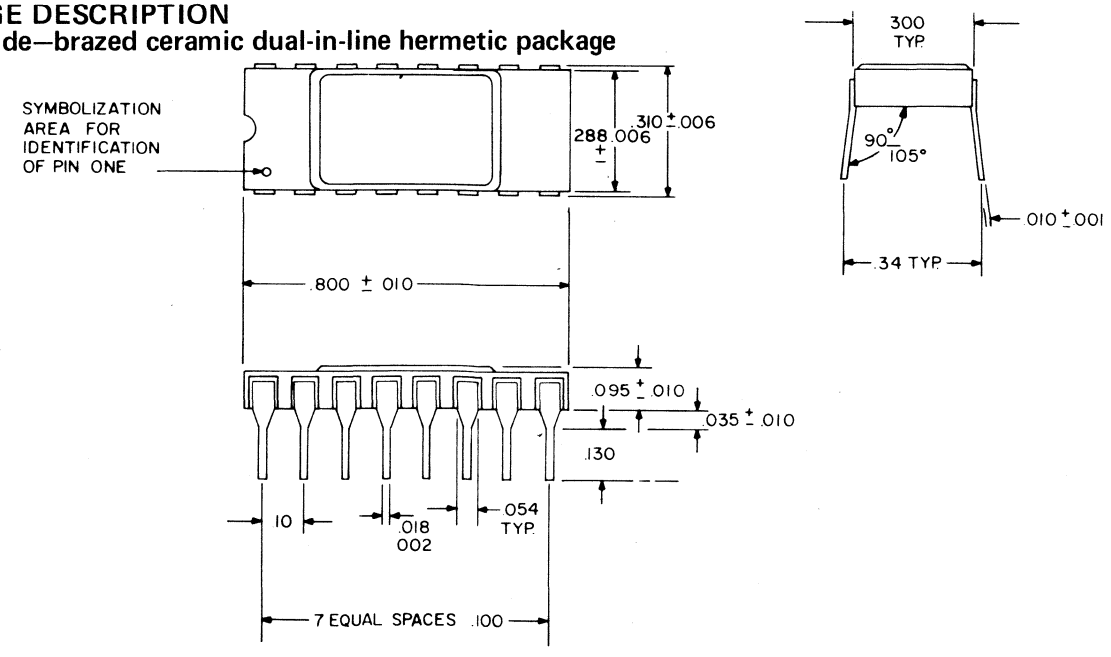


READ-MODIFY-WRITE CYCLE



PACKAGE DESCRIPTION

16-lead side—brazed ceramic dual-in-line hermetic package



PRELIMINARY

MK4200P-16

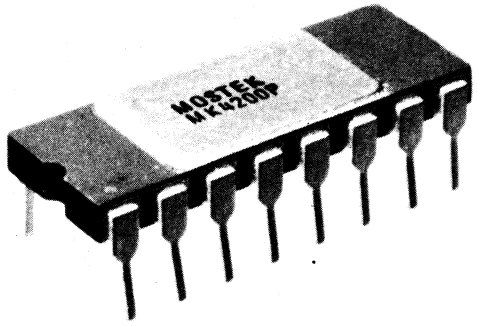
4096 x 1 **BIT DYNAMIC**

MOS Random Access Memory

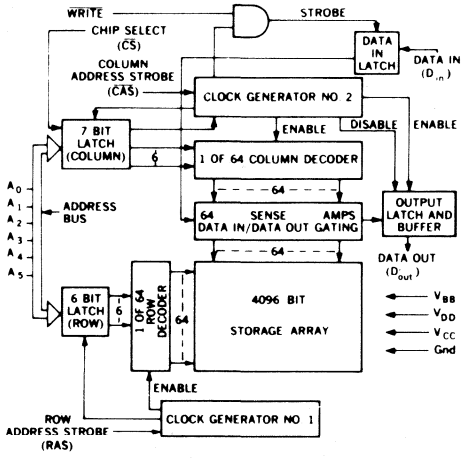
MOSTEK

FEATURES:

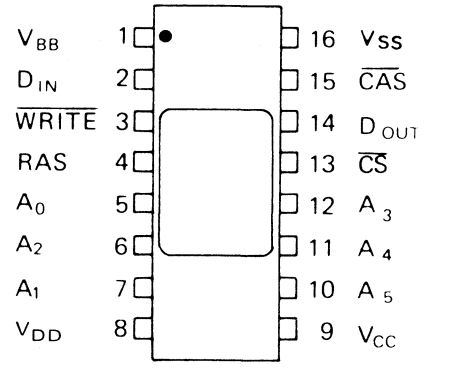
- ☐ Standard 16-pin DIP
- ☐ Inputs protected against static charge
- ☐ All inputs TTL compatible, except RAS
- ☐ On-chip latches for addresses, chip select, and data in
- ☐ Three-state TTL compatible output
- ☐ Chip select decode does not add to access time
- ☐ Output data latched and valid into next cycle
- ☐ Read and write cycles of 425 nsec
- ☐ Access times of 300 nsec
- ☐ Low power: active power under 380 mW
  standby power under .6 mW
- ☐ No power-up sequence required



FUNCTIONAL DIAGRAM



PIN CONNECTIONS



DESCRIPTION:

The MK 4200 is a 4096 x 1 bit dynamic random access memory circuit fabricated with MOSTEK's special Self-Alligned, Poly-Interconnect, N-Channel (SPIN) process to minimize cell area and optimize circuit performance. The single transistor cell uses a dynamic storage technique and each of the 64 row addresses requires refreshing every 2 milliseconds.

A unique multiplexing and latching technique for the address inputs permits the MK 4200 to be packaged in a standard 16-pin DIP on 0.3 each centers. This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

System oriented features on the MK 4200 include very low standby power dissipation, direct interfacing capability with TTL, 6 instead of 12 address lines to drive on-chip registers which can eliminate the need for interface registers, input logic levels selected to optimize the noise immunity, and two chip select methods to allow the user to determine the speed/power characteristics of his memory system.

ADDRESSING:

The 12 address bits required to decode 1 of 4096 cell locations are multiplexed onto the 6 address pins and latched into the on-chip row and column address latches. The Row Address Strobe ($\overline{RAS}$) latches the 6 row address bits into the chip. The Column Address Strobe ($\overline{CAS}$) latches the 6 column address bits plus Chip Select ($\overline{CS}$) into the chip. Since the Chip Select signal is not required until well into the cycle, its decoding time does not add to the system access or cycle time.

ABSOLUTE MAXIMUM RATINGS *

Voltage on any pin relative to V_{BB} ..... -0.5V to +25.0V
Operating Temperature (Ambient) ..... 0° C to 70 °C
Storage Temperature (Ambient) ..... –55 °C to 150°C

RECOMMENDED DC OPERATING CONDITIONS

(0° ≤ T_A ≤ 70 °C)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	11.4	12.0	12.6	volts	1
V_{CC}	Supply Voltage	V_{SS}	5.0	V_{DD}	volts	1,6
V_{SS}	Supply Voltage	0	0	0	volts	1
V_{BB}	Supply Voltage	–4.5	–5.0	–5.5	volts	1
V_{IH}	Logic 1 Voltage, all inputs except $\overline{CAS}$, $\overline{WRITE}$	2.4	5.0	7.0	volts	1,8
V_{IL}	Logic 0 voltage, all inputs	–1.0	0	.8	volts	1,8
V_{IHC}	Logic 1 Voltage $\overline{CAS}$, $\overline{WRITE}$	2.7	5.0	7.0	volts	1,8
V_{IHR}	Logic 1 Voltage, RAS input	V_{DD}–1	12.0	V_{DD}+1	volts	1
V_{ILR}	Logic 0 Voltage, RAS input	–1.0	0.0	+0.6	volts	1

DC ELECTRICAL CHARACTERISTICS

(0 °C ≤ T_A ≤ 70° C) (V_{DD} = 12.0V ± 5%; V_{CC} = 5.0V ± 10%; V_{SS} = 0.V, V_{BB} = –5.0V ± 10%)

	PARAMETER	MIN	MAX	UNITS	NOTES
I_{DDI}	Average V_{DD} Power Supply Current		30	mA	10
I_{CC}	V_{CC} Power Supply Current			mA	3
I_{BB}	Average V_{BB} Power Supply Current		75	μA	
I_{DD2}	Standby V_{DD} Power Supply Current		50	μA	5
$I_{I(L)}$	Input Leakage Current (any input)		10	μA	4
$I_{O(L)}$	Output Leakage Current		10	μA	5
V_{OH}	Output Logic 1 Voltage @ Iout = –5mA	2.4		volts	
V_{OL}	Output Logic 0 Voltage @ Iout = 2 mA		0.4	volts	

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS[14]

($0°C \leq T_A \leq 70°C$) (V_{DD} = 12.0V ± 5%; V_{CC} = 5,0V ± 10%, V_{SS} = 0V, V_{BB} = –5.0V ± 10%)

	PARAMETER	MIN	MAX	UNITS	NOTES
t_{RC}	Random Read or Write Cycle Time	425		nsec	9, 12, 16
t_{RAC}	Access Time from Row Address Strobe		300	nsec	9
t_{CAC}	Access Time from Column Address Strobe		165	nsec	11
t_{OFF}	Output Buffer Turn-Off Delay	0	80	nsec	
t_{RP}	Row Address Strobe Precharge Time	125		nsec	
t_{RCL}	Row to Column Strobe Lead Time	90	135	nsec	11,15
t_{CPW}	Column Address Strobe Pulse Width	165		nsec	
t_{AS}	Address Set-Up Time	0		nsec	
t_{AH}	Address Hold Time	80		nsec	
t_{CH}	Chip Select Hold Time	100		nsec	
t_T	Rise And Fall Times	5	50	nsec	13
t_{RCS}	Read Command Set-Up Time	0		nsec	
t_{RCH}	Read Command Hold Time	0		nsec	
t_{WCH}	Write Command Hold Time	130		nsec	2
t_{WP}	Write Command Pulse Width	130		nsec	
t_{CRL}	Column To Row Strobe Lead Time	–40	+40	nsec	
t_{CWL}	Write Command to Column Strobe Lead Time	165		nsec	7
t_{DS}	Data In Set-Up Time	0		nsec	7
t_{DH}	Data In Hold Time	130		nsec	7
t_{RFSH}	Refresh Period		2	msec	
t_{MOD}	Modify Time	0	10	μsec	

AC ELECTRICAL CHARACTERISTICS [14]

$(0\,^{\circ}C \leq T_A \leq 70\,^{\circ}C)$ $(V_{DD} = 12.0V \pm 5\%, V_{CC} = 5.0 \pm 10\%, V_{SS} = 0V, V_{BB} = -5.0V \pm 10\%)$

	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input Capacitance ($A_0 - A_5$)	6	10	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$ $\overline{CAS}$, D_{IN} $\overline{WRITE}$, $\overline{CS}$)	4	7	pF	
C_O	Output Capacitance (D_{OUT})	5	8	pF	

NOTES:

1. All voltages referenced to V_{SS} .
2. Write Command Hold Time is important only when performing normal random write cycles. During read-write or read modify-write cycles, the Write Command Pulse Width is the limiting parameter.
3. Depends upon output loading. The V_{CC} supply is connected to the output buffer only.
4. All device pins at 0 volts except V_{BB} at -5 volts and pin under test which is at +10 volts.
5. Output disabled by chip select input.
6. Output voltage will swing from V_{SS} to V_{CC} if $V_{CC} \leq V_{DD} - 4$ volts. If $V_{CC} > V_{DD} - 4$ volts. output will swing from V_{SS} to approx. $V_{DD} - 4$ volts.
7. These parameters are referenced to the $\overline{CAS}$ leading edge in random write cycle operation and to the $\overline{WRITE}$ leading edge in read-write or read-modify-write cycles.
8. Input voltages greater than TTL levels (0 to 5V) require device operation at reduced speed.
9. Assumes that $t_{RCL} + t_T \leq t_{RCL\ (max.)}$. If $t_{RCL\ (max.)}$ then t_{RC} and t_{RAC} will be longer by the amount $t_{RCL} + t_T$ exceeds $t_{RCL\ (max.)}$.
10. Current is proportional to speed with maximum current measured at fastest cycle rate.
11. Assumes $t_{RCL} + t_T \geq t_{RCL}$ (max.). If not, the access time is controlled by t_{RAC}.
12. Minimum cycle time is limited by the rise and fall times of the RAS input.
13. Rise and fall time measured between V_{IH} and V_{IL} .
14. Assumes $t_T = 10$ nsec.
15. Max. limit is specified to achieve min. access time
16. Does not account for t_T.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$. The last of these signals making its negative transition is the strobe for the Data In register. This permits several options in the write timing. In a write cycle, if the $\overline{WRITE}$ inputs are brought low prior to $\overline{CAS}$, the Data In is strobed by $\overline{CAS}$ and the set-up and hold time are referenced to this signal. If the cycle is to be a read-write cycle, or read-modify-write cycle, then the $\overline{WRITE}$ input will not go to a logic 0 until after access time. But now, because $\overline{CAS}$ is already at a logic 0, the Data In is strobed in by $\overline{WRITE}$ and the set-up and hold time are referenced to it.

At the beginning of a memory cycle the state of the Data Out Latch and buffer depend on the previous memory cycle. If during the previous cycle the chip was unselected, the output buffer will be in its open-circuit condition. If the previous cycle was a read, read-write, or read-modify-write cycle and the chip was selected, then the output latch and buffer will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. If the previous cycle was a write cycle ($\overline{WRITE}$ active low before access time) and the chip was selected, then the output latch and buffer will contain a logic 1. Regardless of the state of the output it will remain valid until $\overline{CAS}$ goes negative. At that time the output will unconditionally go to its open-circuit state. It will remain open circuit until access time. At access time the output will assume the proper state for the type of cycle performed. If the chip is unselected, it will not accept a $\overline{WRITE}$ command and the output will remain in the open-circuit state.

INPUT/ OUTPUT LEVELS

All inputs to the MK 4200 (except RAS) will interface with TTL. The high impedance, low capacitance input characteristics simplify input driver selection by allowing use of standard logic elements rather than specially designed driver elements. Even though the inputs may be driven directly by TTL gates, pull-up or termination resistors are normally required in a system to prevent ringing of the input signals due to line inductance and reflections. In high speed memory systems, transmission line techniques must be employed on the signal lines to achieve optimum system speeds. Series rather than parallel terminations may be employed at some degradation of system speed.

The RAS input has been specially designed so that very little steady state (D.C.) power is dissipated by the MK 4200 while in standby operation. In doing this, the RAS input requires a high level signal to activate the chip. The ROW ADDRESS STROBE input driver must be able to charge the capacitance load of the RAS input from within 0.6 volt of V_{SS} (0V) to within 1 volt of V_{DD} (+12V) in 50 nanoseconds.

The three-state output buffer is a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS}, for a logic 0. The resistance to V_{CC} is 500-ohms maximum and 150-ohms, typically. The resistance to V_{SS} is 200-ohms maximum and 100-ohms typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During bettery standby operation the V_{CC} pin may be unpowered without affecting the MK 4096P refresh operation. This allows all system logic except the RAS/CAS timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

REFRESH

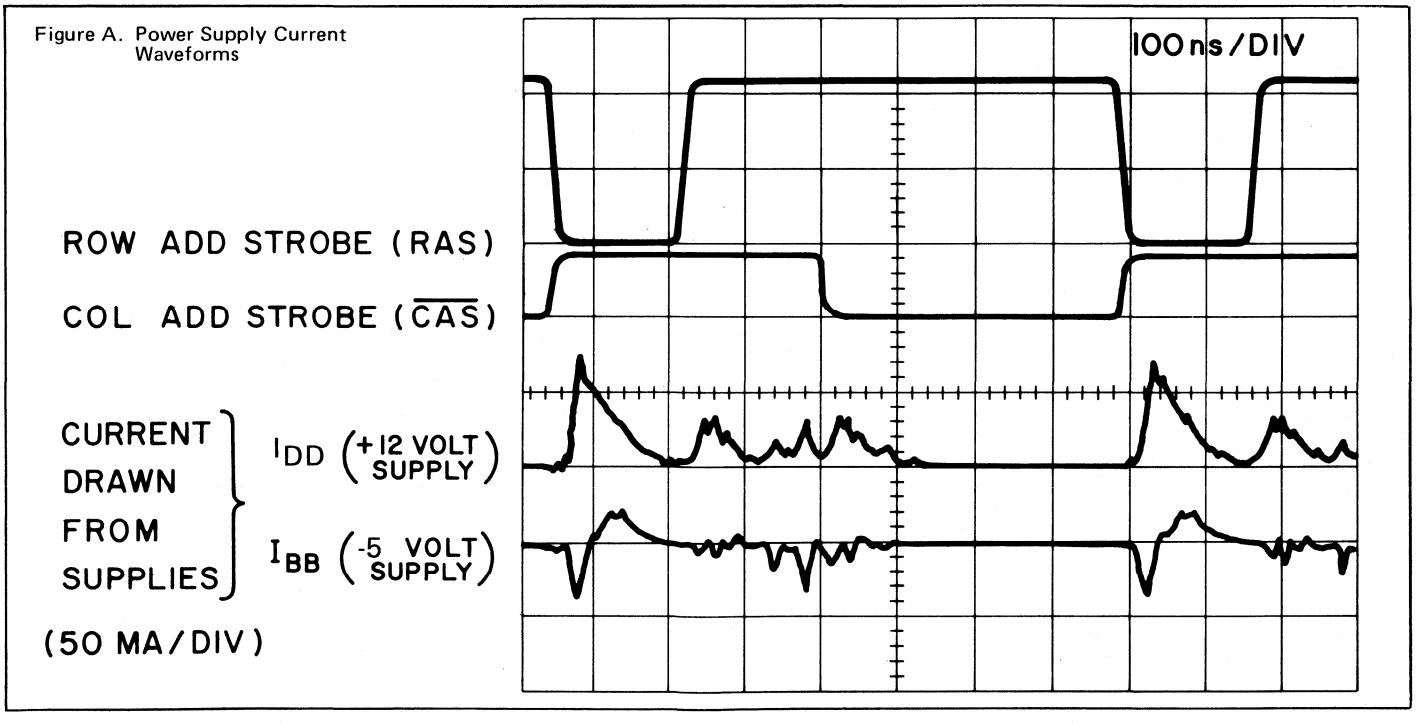
Refresh of the cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses every 2 milliseconds or less. Any read cycle refreshes the selected row, regardless of the state of the Chip Select. A write, read-write, or read-modify-write cycle also refreshes the selected row, but the chip should be unselected to prevent writing data into the selected cell.

POWER DISSIPATION/STANDBY MODE

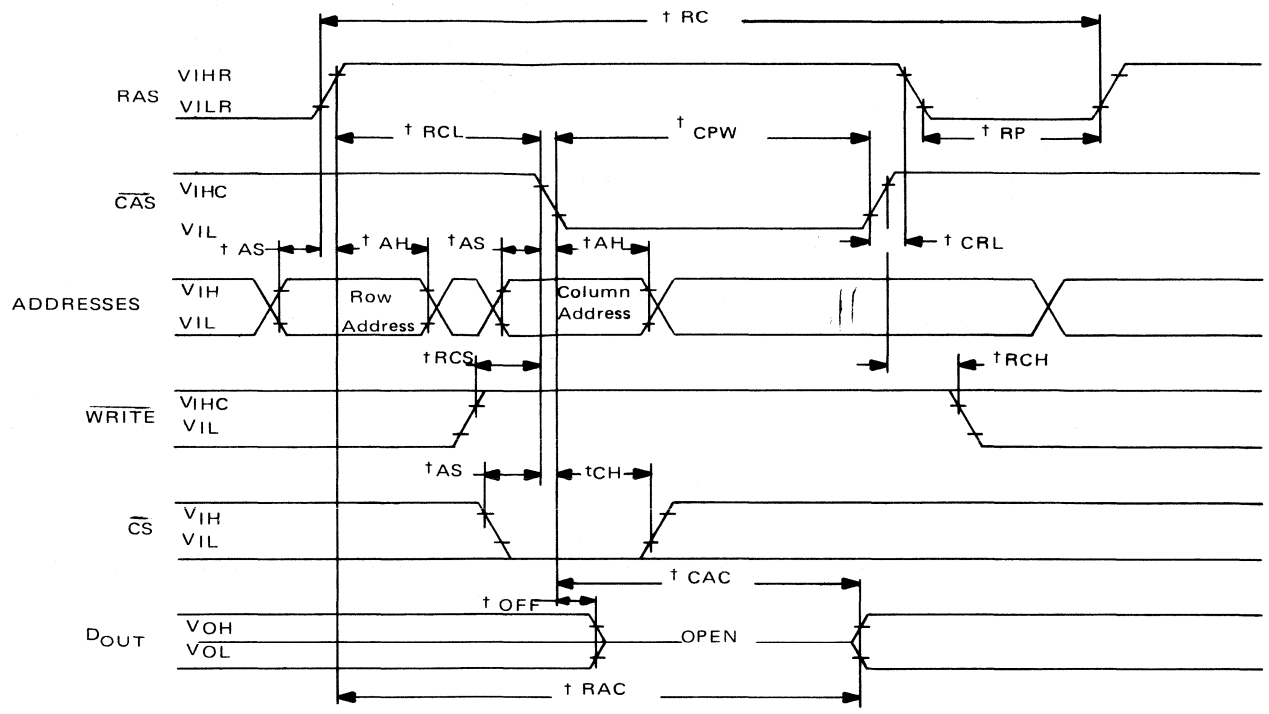
Most of the circuitry used in the MK 4200 is dynamic and draws power only as the result of an address strobe edge. Because the power is not drawn during the whole time the strobe is active, the dynamic power is a function of operating frequency. The power is 120mW at a 1μsec cycle time for the MK 4200P with a worst case power of less than 360 mW at a 425 nsec cycle time. To reduce the overall system power the Row Address Strobe (RAS) must be decoded and supplied to only the selected chips. The $\overline{CAS}$ must be supplied to all chips (to turn off the unselected out-puts). But those chips that did not receive a RAS will not dissipate any power on the $\overline{CAS}$ edges, except for that required to turn off the output. If the RAS is decoded and supplied to the selected chips, then the Chip Select input of all chips can be at a logic 0. The chips that receive a $\overline{CAS}$ but no RAS will be unselected (output open-circuited) regardless of the Chip Select input.

The current waveforms for the current drawn from the V_{DD} and V_{BB} supplies are shown in Figure A. Since the current is pulsed, proper power distribution and bypassing techniques are required to maintain system power supply noise levels at an acceptable level. Low inducatance supply lines for V_{DD} and V_{SS} are desirable. A minimum of one 0.01 microfarad, low inductance, bypass capacitance per two MK 4200P devices and one 6.8 microfarad electrolytic capacitor per eight MK 4200P devices on each of the V_{DD} and V_{BB} supply lines is desirable.

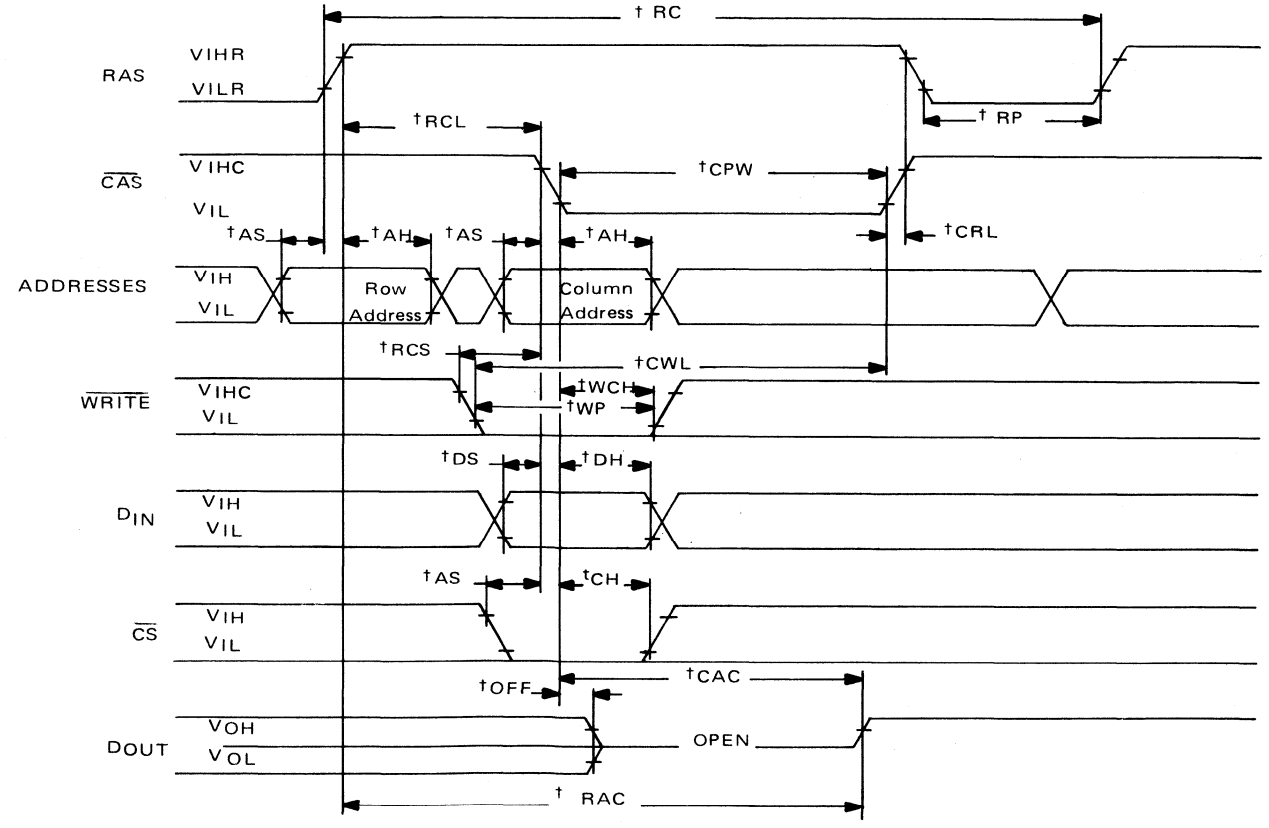
Figure A. Power Supply Current Waveforms



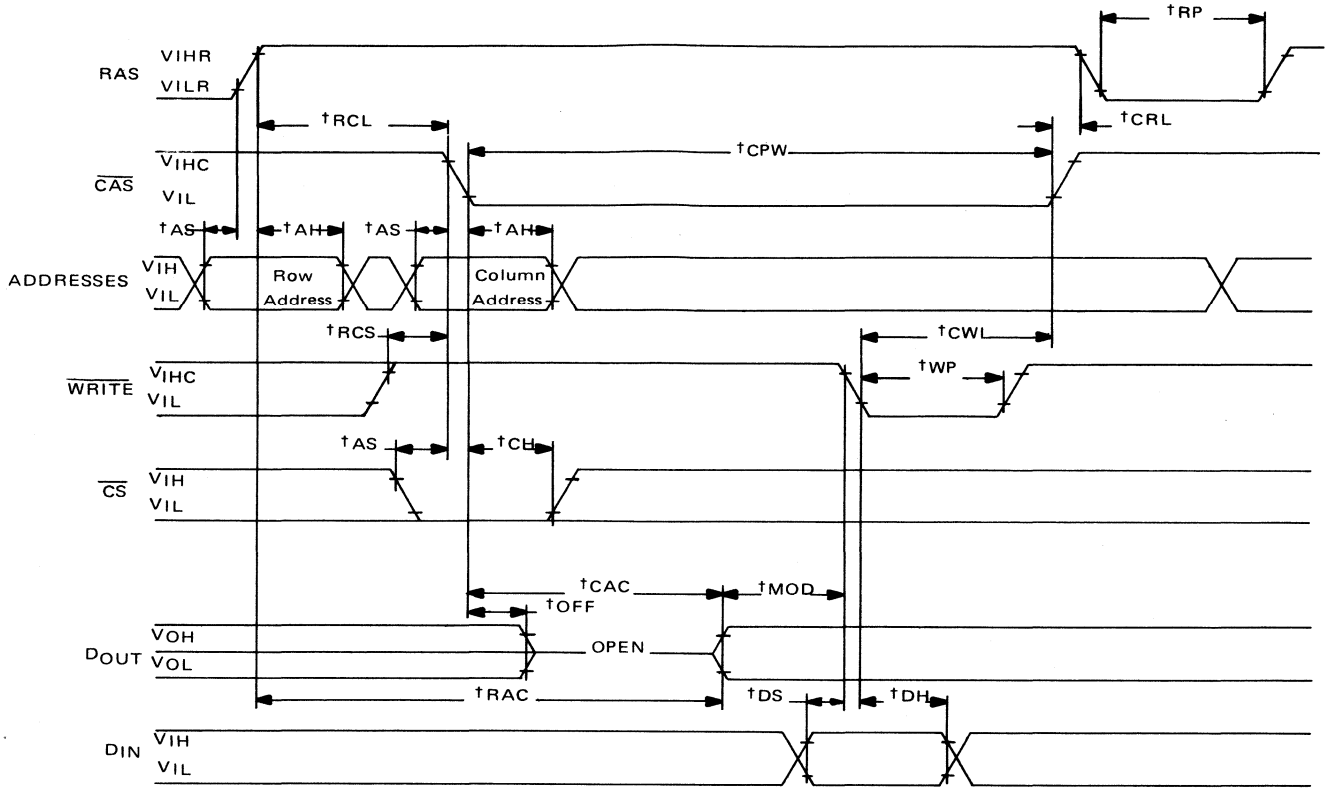
READ CYCLE



WRITE CYCLE

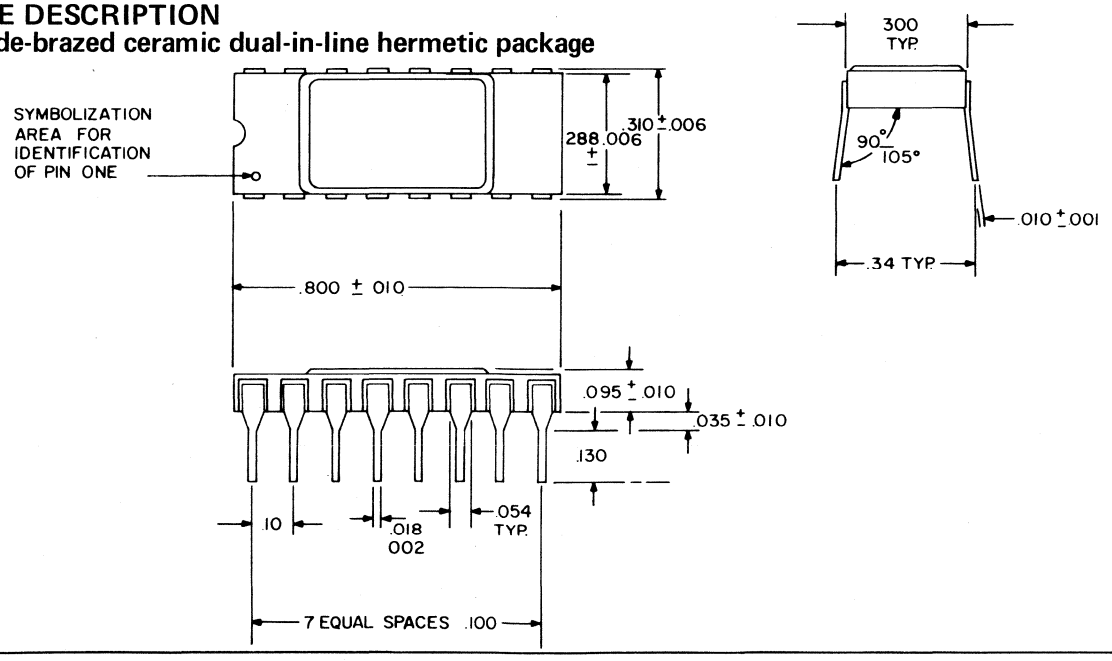


READ-MODIFY-WRITE CYCLE



PACKAGE DESCRIPTION

16-lead side-brazed ceramic dual-in-line hermetic package



MEMORIES

MICRO-PROCESSORS

CONSUMER

CIRCUITS

INDUSTRIAL

FUTURE PRODUCTS

MOSTEK

THE F8 FROM MOSTEK...

A UNIVERSAL STANDARD MICROPROCESSOR

VERSATILE . . EFFICIENT . . COST EFFECTIVE

The ultimate goal, from F8 design concept through development and production, was to produce the most versatile, efficient, cost-effective microprocessor system available today. To accomplish this, five stringent parameters, based on user experience with other systems, were set forth as guidelines for the F8.

- Minimum Parts Count
- Cost Effectiveness
- Simple Peripheral Interfaces
- Easy Expansion through Modular Architecture
- Simplified Programming and Debugging

HOW WERE F8 GOALS MET ?

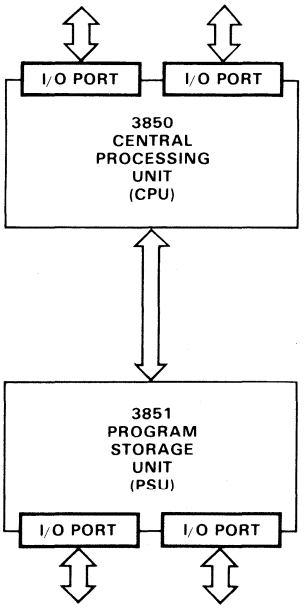
By . . . unique system partitioning the system functions have been divided among the various circuits of the F8 family to provide sophisticated modularity. As a result, it is now possible to build a minimum microprocessor system with **only two devices.** To this system, PSU, RAM and I/O devices can be added to form medium size or memory intensive systems with a minimum use of external parts. And, finally, for solving complex problems, the F8 devices can be connected as subsystems into a synergistic system of independent microprocessors.

By . . . incorporating the I/O structure on the chips so that the majority (95%) of the peripheral devices can be directly controlled without the need for special circuits. The trick is to accommodate the characteristics of a given peripheral device in the software. The I/O hardware structure includes a programmable timer, an efficient interrupt system and bidirectional I/O ports.

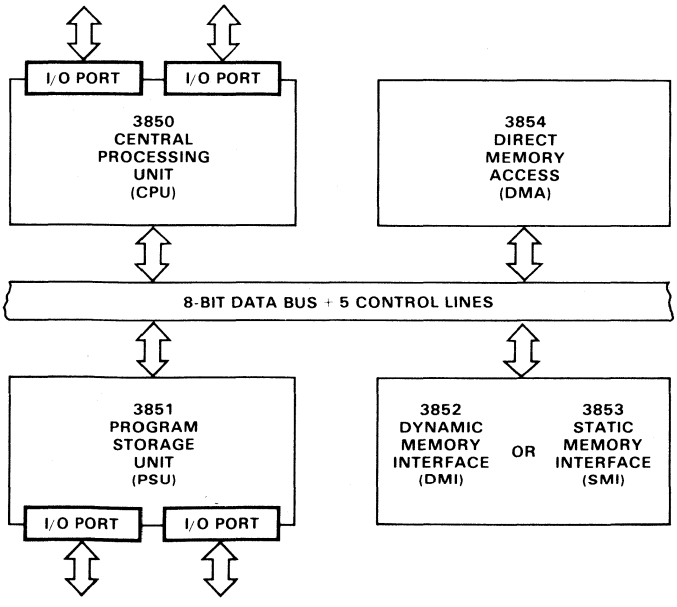
By . . . providing carefully thought out support software and hardware for generating and debugging microprograms.

WHAT IS THE RESULT ?

. . . a complete family of LSI circuits that can be used as building blocks to construct versatile, efficient, cost effective systems from the most simple to the highly complex.

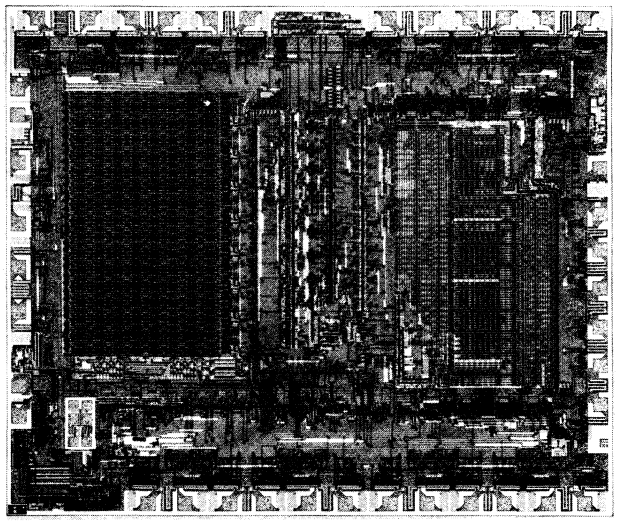


MINIMUM SYSTEM

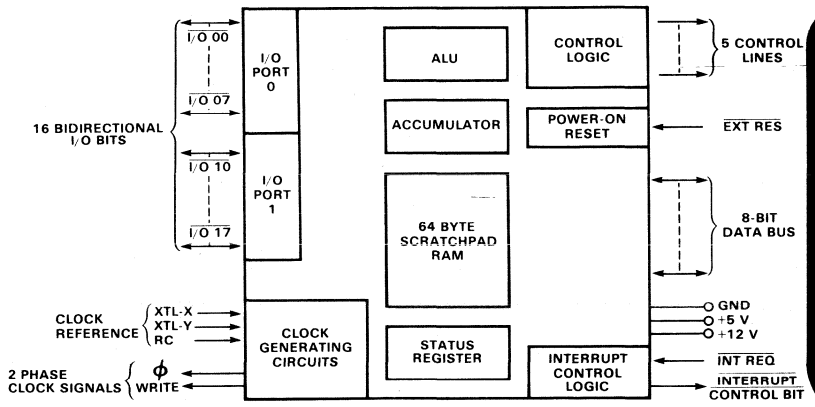


F8 DEVICE FAMILY

MK 3850 CENTRAL PROCESSING UNIT

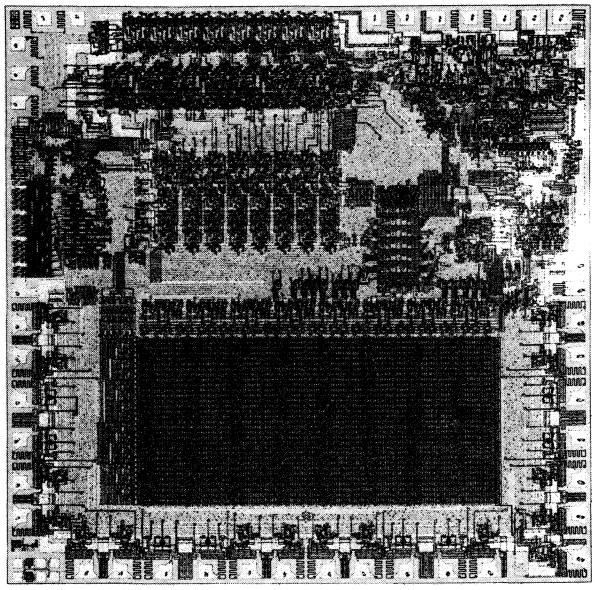


MOSTEK's F8 Central Processing Unit (CPU) contains all of the functions of an ordinary central processor and adds some time and money saving features uniquely its own. For instance, the 64 bytes of scratchpad RAM memory already included on the F8 CPU eliminate the need for external RAM circuits in many applications. Clock and power-on-reset circuitry, normally requiring additional integrated circuit packages, are included on-chip. MOSTEK's CPU also contains 16 bits of fully bidirectional input and output lines internally latched (for storing output data) and capable of driving a standard TTL load.



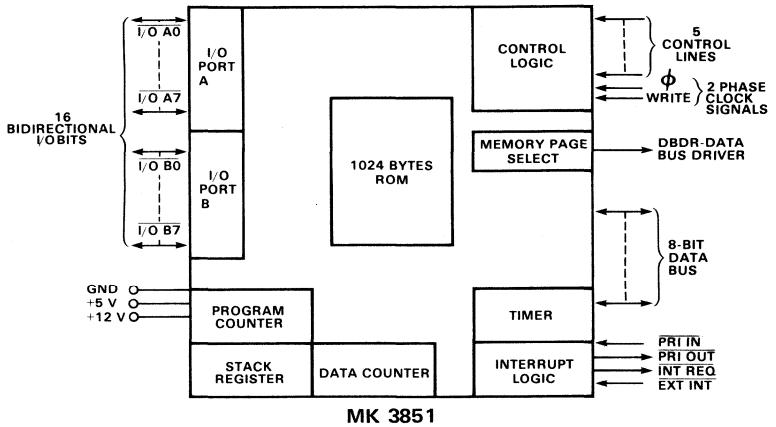
MK 3850
CPU BLOCK DIAGRAM

MK 3851 PROGRAM STORAGE UNIT

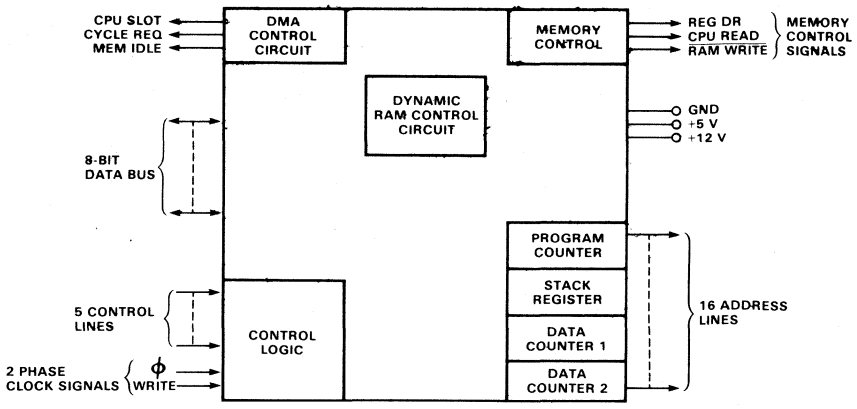


It is important to note that MOSTEK's Program Storage Unit (PSU) is not just a conventional Read Only Memory. In addition to containing 1024 bytes of mask programmable ROM for program and constant storage, the F8 PSU includes the addressing logic for memory referencing, a Program Counter, an Indirect Address Register (the Data Counter) and a Stack Register. A complete vectored interrupt level, including an external interrupt line to alert the central processor, is provided All of the logic necessary to request, acknowledge and reset the interrupt is on the F8 PSU. The 8-bit Programmable Timer is especially useful for generating real time delays. The PSU has an additional 16 bits of TTL compatible, bidirectional, fully latched I/O lines.

Systems requiring more program storage may be expanded by adding more PSU circuits. For example, one F8 CPU and three F8 PSUs will produce a microprocessor system complete with 64 bytes of RAM, 3072 bytes of ROM, 64 I/O bits, three interrupt levels, and three programmable timers. This complete system will require only four IC packages.



MK 3851
PSU BLOCK DIAGRAM

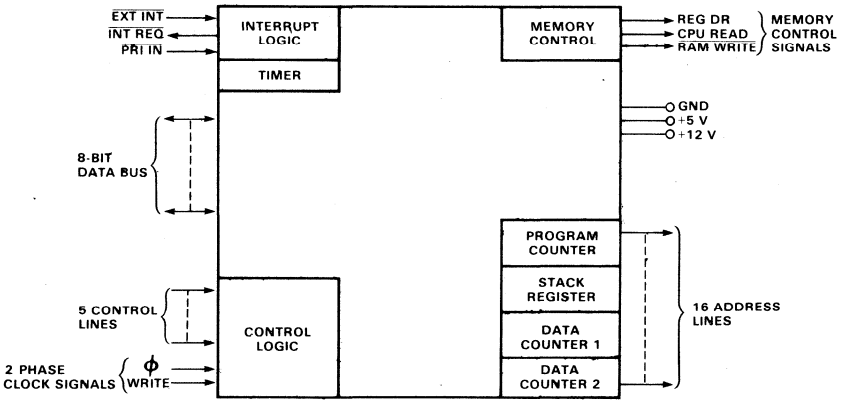


MK 3852
DMI BLOCK DIAGRAM

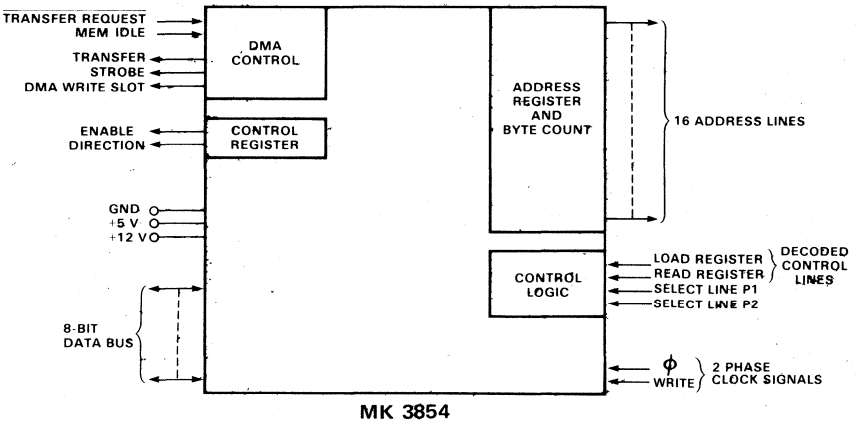
MK 3852/MK 3853 MEMORY INTERFACE

For applications requiring more than the 64 byte RAM located on the CPU, two memory interface circuits are included in the F8 set. Each device generates the 16 address lines and the signals necessary to interface with up to 65K bytes of RAM, PROM or ROM memory. Either device may be used in conjunction with standard static semiconductor memory devices.

The Static Memory Interface (SMI) contains a full level of interrupt capability and a programmable timer. The Dynamic Memory Interface (DMI) contains all of the logic necessary to refresh MOS dynamic memories without degrading the system throughput time. The F8 DMI can also interface with static memories when desired.



MK 3853
SMI BLOCK DIAGRAM



MK 3854
DMA BLOCK DIAGRAM

MK 3854 DIRECT MEMORY ACCESS

MOSTEK's Direct Memory Access (DMA) device sets up a high speed data path to link F8 memory with peripheral electronics. The F8 DMA circuit, when working in conjunction with the F8 DMI, does not require overhead electronics to keep track of memory addresses; bytes transferred and handshaking signals. The data transfer is initiated by the CPU under program control. Once started, the DMA transfer will continue without CPU intervention. The CPU can sense the enable line of the DMA to determine the completion of a transfer. The entire DMA transfer will take place without halting the central processor.

F8 MICROPROCESSOR SYSTEMS

A TWO-CIRCUIT SYSTEM

The two-circuit F8 microprocessor is suitable for small data terminals, controllers, and specialty calculators. The keyboard is connected directly to the F8 I/O ports without special interfaces. Switch-bounce protection, rollover, and key encoding are all under software control. Software also decodes signals for LED readouts.

As an appliance controller, for example, the two-circuit system can perform all input-output sensing, actuating, timing, and computation operations. A system like the combination washing-machine-and-dryer controller in *Figure 1* requires more than 250 components when other microprocessor device sets are used, but with the F8 devices uses only 55 components, including 28 LEDs and the power semiconductor devices and relays used to control the motors. A set of custom circuits would also require about 50 parts, but initial engineering expense is heavy and severe penalties are incurred if changes are required. With the F8 system changes can be made by merely changing the program.

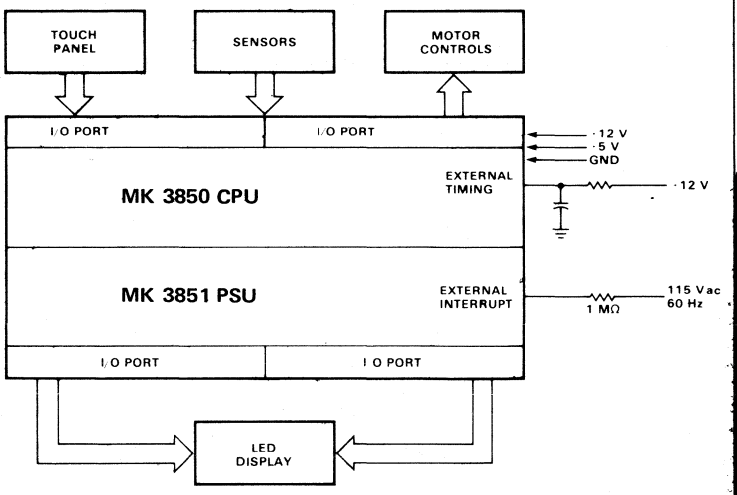


Fig. 1. Two-Circuit System

A MORE COMPLEX SYSTEM

The versatility of the F8 system is indicated by the traffic-light-controls system in *Figure 2*. The use of one CPU and two PSU circuits provides the designer with two timers, two interrupts, an onboard clock, onboard power-on reset, onboard switch decoding, and 48 bidirectional I/O bits. This system could be tied to vehicle detectors in the road, to monitor traffic for left-turn lanes as well as through-traffic flow in four directions. It would also react to interrupts from the pedestrian control buttons at each corner. There also is sufficient I/O capability to permit communication with and control of neighboring intersections and to allow the system to be operated manually or tested for proper operation.

Five F8 features are of particular interest for this type of application. One of the interrupts can eliminate the need for such external circuits as a comparator to compare a count of the cars with a predetermined value to cause the light to change. (The CPU can handle the simple arithmetic of counting cars.) This interrupt also eliminates the need for continuous polling of traffic count by the microcomputer. The second interrupt would be ideal for permitting pedestrian control to override the automatic system. The internal clock, with an external crystal, can also control light routines.

The two timers permit simultaneous counting of delay for vehicle signals and flashing warning lights for pedestrians. The onboard power-on reset acts in case of power failure to start the system automatically when power is renewed. The bidirectional I/Os have built-in latches that eliminate the need for external latches for the job of "holding" commands for lights as well as the momentary commands provided by timers and sensors.

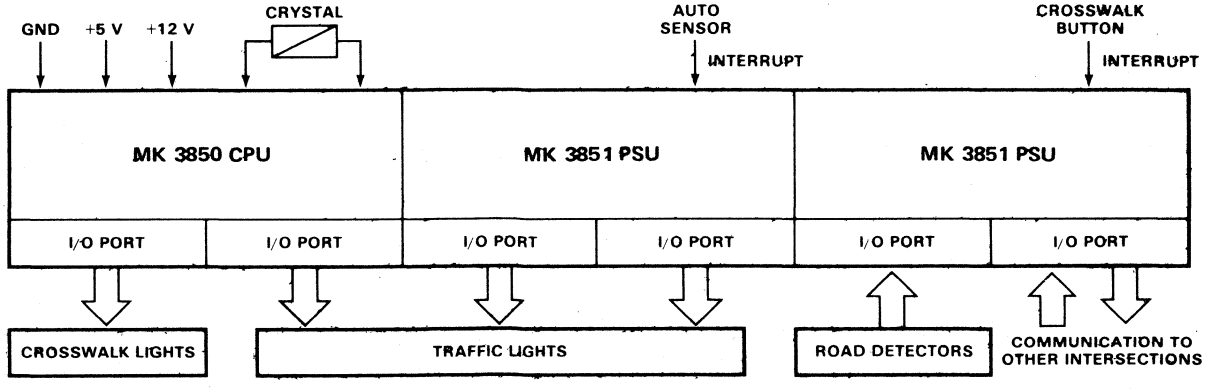


Fig. 2. Medium Complexity System

A MEMORY INTENSIVE SYSTEM

A typical application is a printing credit-verification terminal *(Figure 3)*. Such a system requires high performance and yet must be low in cost if it is to reach a large market. Only four different F8 devices are required to handle a keyboard input, visual display, card reader, and printer as well as provide a modem interface and memory interface for external RAM storage. This printing credit-verification system might be compared to a "bare mini-computer" in terms of utility, however, a detailed engineering evaluation would show that it costs less, has fewer parts and a more flexible I/O structure.

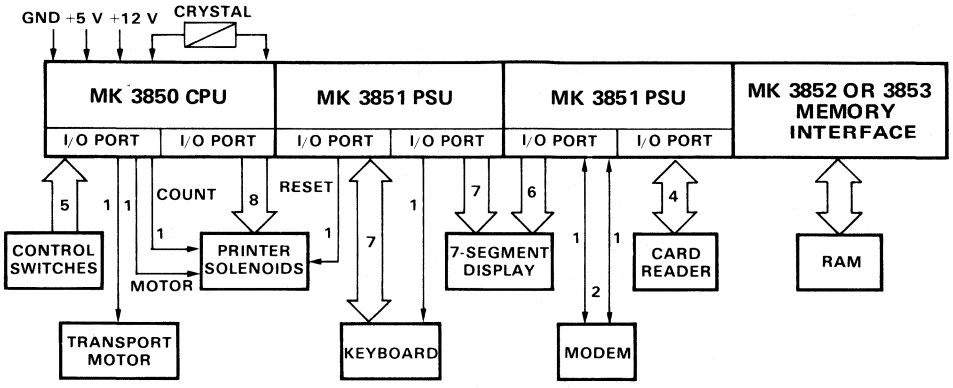


Fig. 3. Memory Intensive System

MULTI-MICROPROCESSOR SYSTEM

Figure 4 shows a specific application of the multi-processing concept as applied to a keyboard-to-floppy-disk system. Possibly this is the most cost-effective way of implementing this system, conservatively costing less than 50% of a conventional implementation. This system involves concurrent operation of three floppy disks, magnetic tape, CRT, keyboard, printer, and modem. While the low-speed devices (the keyboard, printer, and modem) can be adequately handled by the programmed I/O structure, the high-speed devices (disks, magnetic tape, and CRT) require separate F8 CPUs and PSUs.

This scheme provides simplicity of control, modularity, and freedom to expand. In this case, the units operating concurrently are: one magnetic-tape unit (25 μs/byte); three floppy-disk units (32 μs/byte each); and a CRT unit (71 μs/byte). This combination requires an aggregate bandwidth of 0.1478 byte/μs. This is well within the F8's upper bandwidth limit of 0.5 byte/μs.

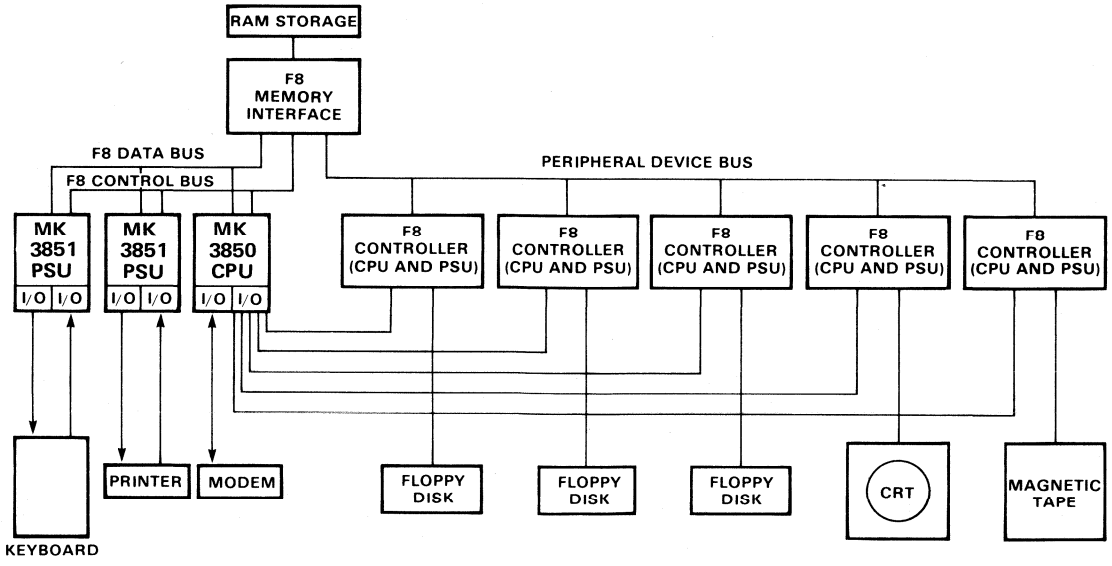


Fig. 4. Multi Microprocessor System

F8 INSTRUCTION SET SUMMARY

The F8 instruction set contains over 60 different instructions which may be subdivided into 10 categories: Accumulator, Scratchpad Register, Indirect Scratchpad Address Register, Memory Reference, Data Counter, Status Register, Program Counter, Branch, Interrupt Control and Input/Output instructions. Because 55% of the F8 instructions are only one byte long, programs are short and memory requirements significantly reduced. An alphabetic listing of the instructions is shown below. The following pages contain a complete description of the F8 instructions, including the cycle time. Each cycle is 2 μs for a system with a 2 MHz clock frequency.

F8 ADDRESSING MODES

The F8 instruction set has eight modes of referencing either I/O, CPU registers or bulk memory.

Implied Addressing – The data for this one-byte instruction is implied by the actual instruction. For example, the POP instruction automatically implies that the content of the Program Counter will be set to the value contained in the Stack Register.

Direct Addressing – In these two-byte instructions, the address of the operand is contained in the second byte of the instruction. The Direct Addressing mode is used in the Input/Output class of instructions.

Short Immediate Addressing – Instructions whose addressing mode is Short Immediate have the instruction op code as the first four bits and the operand as the last four bits. They are all one-byte instructions.

Long Immediate Addressing – In these two-byte instructions, the first instruction byte is the op code and the second byte is the 8-bit operand.

Direct Register Addressing – This mode of addressing may be used to directly reference the Scratchpad Registers. By including the register number in the one-byte instruction, 12 of the 64 Scratchpad Registers may be referenced directly.

Indirect Register Addressing – All 64 Scratchpad Registers may be indirectly referenced, using the Indirect Scratchpad Register in the CPU. This 6-bit register, which acts as a pointer to the scratchpad memory, may either be incremented, decremented, or left unchanged while accessing the scratchpad register.

Indirect Memory Addressing – A 16-bit Indirect Address Register, the Data Counter, points to either data or constants in bulk memory. A group of one-byte instructions is provided to manipulate this area of memory. These instructions imply that the Data Counter is pointing to the desired memory byte. The Data Counter is self-incrementing, allowing for an entire data field to be scanned and manipulated without requiring special instructions to increment its content. The memory interface circuit contains two interchangeable data counters.

Relative Addressing – All F8 Branch Instructions use the relative addressing mode. Whenever a branch is taken, the Program Counter is updated by an 8-bit relative address contained in the second byte of the instruction. A branch may extend 128 locations forward or 127 locations back.

ALPHABETIC LIST OF INSTRUCTIONS

ADC	Add Data Counter with Accumulator
AI	Add Immediate with Accumulator
AM	Add Binary Accumulator with Memory
AMD	Add Decimal Accumulator with Memory
AS	Add Binary Accumulator with Scratchpad Register
ASD	Add Decimal Accumulator with Scratchpad Register
BC	Branch on Carry
BF	Branch on False Condition
BM	Branch if Negative
BNC	Branch if no Carry
BNO	Branch if no Overflow
BNZ	Branch if no Zero
BP	Branch if Positive
BR	Absolute Branch
BR7	Branch if ISAR is not 7
BT	Branch on True Condition
BZ	Branch on Zero Condition
CI	Compare Immediate
CLR	Clear Accumulator
CM	Compare with Memory
COM	Complement Accumulator
DCI	Load Data Counter Immediate
DI	Disable Interrupt
DS	Decrement Scratchpad Register
EI	Enable Interrupt
INC	Increment Accumulator
IN	Input
INS	Input Short
JMP	Jump
LI	Load Accumulator Immediate
LIS	Load Accumulator Short
LISL	Load ISAR – Lower 3 Bits
LISU	Load ISAR – Upper 3 Bits
LM	Load Memory
LNK	Link Carry into Accumulator
LR	Load Register (5 Types) Scratchpad Program Counter ISAR Status Data Counter
NI	Logical AND Accumulator Immediate
NM	Logical AND Memory Accumulator
NOP	No Operation
NS	Logical AND Scratchpad and Accumulator
OI	Logical OR Immediate
OM	Logical OR Memory with Accumulator
OUT	Output
OUTS	Output Short
PI	Push Program Counter into Stack Register Set Program Counter to New Location
PK	Push Program Counter into Stack Register Set Program Counter from Scratchpad
POP	Put Stack Register into Program Counter
SL	Shift Left
SR	Shift Right
ST	Store Memory
XDC	Exchange Data Counters
XI	Exclusive OR Immediate
XM	Exclusive OR Accumulator with Memory
XS	Exclusive OR Accumulator with Scratchpad

ACCUMULATOR GROUP INSTRUCTIONS

OPERATION	MNEMONIC OP CODE	OPERAND	FUNCTION	MACHINE CODE	BYTES	CYCLES	STATUS BITS OVF	ZERO	CRY	SIGN
ADD CARRY	LNK		ACC←(ACC) + CRY	19	1	1	1/0	1/0	1/0	1/0
ADD IMMEDIATE	AI	ii	ACC←(ACC) + H'ii'	24ii	2	2.5	1/0	1/0	1/0	1/0
AND IMMEDIATE	NI	ii	ACC←(ACC) ∧ H'ii'	21ii	2	2.5	0	1/0	0	1/0
CLEAR	CLR		ACC←H'00'	70	1	1	–	–	–	–
COMPARE IMMEDIATE	CI	ii	H'ii' + $(\overline{ACC})$ + 1	25ii	2	2.5	1/0	1/0	1/0	1/0
COMPLEMENT	COM		ACC←(ACC) ⊕ H'FF'	18	1	1	0	1/0	0	1/0
EXCLUSIVE-OR IMMEDIATE	XI	ii	ACC←(ACC) ⊕ H'ii'	23ii	2	2.5	0	1/0	0	1/0
INCREMENT	INC		ACC←(ACC) + 1	1F	1	1	1/0	1/0	1/0	1/0
LOAD IMMEDIATE	LI	ii	ACC←H'ii'	20ii	2	2.5	–	–	–	–
LOAD IMMEDIATE SHORT	LIS	i	ACC←H'0i'	7i	1	1	–	–	–	–
OR IMMEDIATE	OI	ii	ACC←(ACC) ∨ H'ii'	22ii	2	2.5	0	1/0	0	1/0
SHIFT LEFT ONE	SL	1	SHIFT LEFT 1	13	1	1	0	1/0	0	1/0
SHIFT LEFT FOUR	SL	4	SHIFT LEFT 4	15	1	1	0	1/0	0	1/0
SHIFT RIGHT ONE	SR	1	SHIFT RIGHT 1	12	1	1	0	1/0	0	1
SHIFT RIGHT FOUR	SR	4	SHIFT RIGHT 4	14	1	1	0	1/0	0	1

BRANCH INSTRUCTIONS

In all conditional branches $PC_0 \leftarrow (PC_0) + 2$ if the test condition is not met. Execution is complete in 3.0 cycles.

OPERATION	MNEMONIC OP CODE	OPERAND	FUNCTION	MACHINE CODE	BYTES	CYCLES	STATUS BITS OVF	ZERO	CRY	SIGN
BRANCH ON CARRY	BC	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if CRY = 1	82aa	2	3.5	–	–	–	–
BRANCH ON POSITIVE	BP	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if SIGN = 1	81aa	2	3.5	–	–	–	–
BRANCH ON ZERO	BZ	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if ZERO = 1	84aa	2	3.5	–	–	–	–
BRANCH ON TRUE	BT	taa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if any test is true t = TEST CONDITION	8taa	2	3.5	–	–	–	–
BRANCH IF NEGATIVE	BM	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if SIGN = 0	91aa	2	3.5	–	–	–	–
BRANCH IF NO CARRY	BNC	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if CARRY = 0	92aa	2	3.5	–	–	–	–
BRANCH IF NO OVERFLOW	BNO	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if OVF = 0	98aa	2	3.5	–	–	–	–
BRANCH IF NOT ZERO	BNZ	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if ZERO = 0	94aa	2	3.5	–	–	–	–
BRANCH IF FALSE TEST	BF	taa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if all false test bits t = TEST CONDITION	9taa	2	3.5	–	–	–	–
BRANCH IF ISAR (LOWER) ≠ 7	BR7	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if ISARL ≠ 7 $PC_0 \leftarrow (PC_0) + 2$ if ISARL = 7	8Faa	2	2.5 2.0	– –	– –	– –	– –
BRANCH RELATIVE	BR	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$	90aa	2	3.5	–	–	–	–
JUMP*	JMP	aaaa	$PC_0 \leftarrow H'aaaa'$	29aaaa	3	5.5	–	–	–	–

2^2	2^1	2^0
ZERO	CRY	SIGN

2^3	2^2	2^1	2^0
OVF	ZERO	CRY	SIGN

*Privileged instruction

MEMORY REFERENCE INSTRUCTIONS

In all Memory Reference Instructions, the Data Counter is incremented DC←DC + 1.

OPERATION	MNEMONIC OP CODE	OPERAND	FUNCTION	MACHINE CODE	BYTES	CYCLES	STATUS BITS OVF	ZERO	CRY	SIGN
ADD BINARY	AM		ACC←(ACC)+[(DC)]	88	1	2.5	1/0	1/0	1/0	1/0
ADD DECIMAL	AMD		ACC←(ACC)+[(DC)]	89	1	2.5	1/0	1/0	1/0	1/0
AND	NM		ACC←(ACC)∧[(DC)]	8A	1	2.5	0	1/0	0	1/0
COMPARE	CM		[(DC)]+($\overline{ACC}$) + 1	8D	1	2.5	1/0	1/0	1/0	1/0
EXCLUSIVE OR	XM		ACC←(ACC)⊕[(DC)]	8C	1	2.5	0	1/0	0	1/0
LOAD	LM		ACC←[(DC)]	16	1	2.5	–	–	–	–
LOGICAL OR	OM		ACC←(ACC)∨[(DC)]	8B	1	2.5	0	1/0	0	1/0
STORE	ST		(DC)←(ACC)	17	1	2.5	–	–	–	–

ADDRESS REGISTER GROUP INSTRUCTIONS

OPERATION	MNEMONIC OP CODE	OPERAND	FUNCTION	MACHINE CODE	BYTES	CYCLES	STATUS BITS OVF	ZERO	CRY	SIGN
ADD to DATA COUNTER	ADC		DC←(DC) + (ACC)	8E	1	2.5	–	–	–	–
CALL to SUBROUTINE*	PK		PC_0U←(r12); PC_0L←(r13); PC_1←(PC_0)	0C	1	4	–	–	–	–
CALL to SUBROUTINE IMMEDIATE*	PI	aaaa	PC_1←(PC_0); PC_0←H'aaaa	28aaaa	3	6.5	–	–	–	–
EXCHANGE DC	XDC		$DC_0 \rightleftarrows DC_1$	2C	1	2	–	–	–	–
LOAD DATA COUNTER	LR	DC,Q	DCU←(r14); DCL←(r15)	0F	1	4	–	–	–	–
LOAD DATA COUNTER	LR	DC,H	DCU←(r10); DCL←(r11)	10	1	4	–	–	–	–
LOAD DC IMMEDIATE	DCI	aaaa	DC←H'aaaa'	2Aaaaa	3	6	–	–	–	–
LOAD PROGRAM COUNTER	LR	PO,Q	PC_0U←(r14); PC_0L←(r15)	0D	1	4	–	–	–	–
LOAD STACK REGISTER	LR	P,K	PC_1U←(r12); PC_1L←(r13)	09	1	4	–	–	–	–
RETURN FROM SUBROUTINE*	POP		PC_0←(PC_1)	1C	1	2	–	–	–	–
STORE DATA COUNTER	LR	Q,DC	r14←(DCU); r15←(DCL)	0E	1	4	–	–	–	–
STORE DATA COUNTER	LR	H,DC	r10←(DCU); r11←(DCL)	11	1	4	–	–	–	–
STORE STACK REGISTER	LR	K,P	r12←(PC_1U); r13←(PC_1L)	08	1	4	–	–	–	–

SCRATCHPAD REGISTER INSTRUCTIONS

(Refer to Scratchpad Addressing Modes)

OPERATION	MNEMONIC OP CODE	OPERAND	FUNCTION	MACHINE CODE	BYTES	CYCLES	STATUS BITS OVF	ZERO	CRY	SIGN
ADD BINARY	AS	r	ACC←(ACC) + (r)	Cr	1	1	1/0	1/0	1/0	1/0
ADD DECIMAL	ASD	r	ACC←(ACC) + (r)	Dr	1	2	1/0	1/0	1/0	1/0
DECREMENT	DS	r	r←(r) + H'FF'	3r	1	1.5	1/0	1/0	1/0	1/0
LOAD	LR	A,r	ACC←(r)	4r	1	1	–	–	–	–
LOAD	LR	A,KU	ACC←(r12)	00	1	1	–	–	–	–
LOAD	LR	A,KL	ACC←(r13)	01	1	1	–	–	–	–
LOAD	LR	A,QU	ACC←(r14)	02	1	1	–	–	–	–
LOAD	LR	A,QL	ACC←(r15)	03	1	1	–	–	–	–
LOAD	LR	r,A	r←(ACC)	5r	1	1	–	–	–	–
LOAD	LR	KU,A	r12←(ACC)	04	1	1	–	–	–	–
LOAD	LR	KL,A	r13←(ACC)	05	1	1	–	–	–	–
LOAD	LR	QU,A	r14←(ACC)	06	1	1	–	–	–	–
LOAD	LR	QL,A	r15←(ACC)	07	1	1	–	–	–	–
AND	NS	r	ACC←(ACC) ∧ (r)	Fr	1	1	0	1/0	0	1/0
EXCLUSIVE OR	XS	r	ACC←(ACC) ⊕ (r)	Er	1	1	0	1/0	0	1/0

*Privileged instruction

MISCELLANEOUS INSTRUCTIONS

OPERATION	MNEMONIC OP CODE	OPERAND	FUNCTION	MACHINE CODE	BYTES	CYCLES	STATUS BITS OVF	ZERO	CRY	SIGN
DISABLE INTERRUPT	DI		RESET ICB	1A	1	2	–	–	–	–
ENABLE INTERRUPT*	EI		SET ICB	1B	1	2	–	–	–	–
INPUT	IN	aa	ACC←(INPUT PORT aa)	26aa	2	4	0	1/0	0	1/0
INPUT SHORT	INS	a	ACC←(INPUT PORT a)	Aa	1	4***	0	1/0	0	1/0
LOAD ISAR	LR	IS,A	ISAR←(ACC)	0B	1	1	–	–	–	–
LOAD ISAR LOWER	LISL	a	ISARL←a	1101a**	1	1	–	–	–	–
LOAD ISAR UPPER	LISU	a	ISARU←a	01100a**	1	1	–	–	–	–
LOAD STATUS REGISTER*	LR	W,J	W←(r9)	1D	1	2	1/0	1/0	1/0	1/0
NO-OPERATION	NOP		PC_0←(PC_0) + 1	2B	1	1	–	–	–	–
OUTPUT	OUT	aa	OUTPUT PORT aa←(ACC)	27aa	2	4	–	–	–	–
OUTPUT SHORT	OUTS	a	OUTPUT PORT a←(ACC)	Ba	1	4***	–	–	–	–
STORE ISAR	LR	A,IS	ACC←(ISAR)	0A	1	1	–	–	–	–
STORE STATUS REG	LR	J,W	r9←(W)	1E	1	1	–	–	–	–

*Privileged instruction
**3-bit octal digit
***2 machine cycles for CPU ports

NOTES.

Each lower case character represents a Hexadecimal digit
Each cycle equals 4 machine clock periods
Lower case denotes variables specified by programmer

Function Definitions

←	is replaced by
( )	the contents of
(–)	Binary "1"s complement of
+	Arithmetic Add (Binary or Decimal)
⊕	Logical "OR" exclusive
∧	Logical "AND"
∨	Logical "OR" inclusive
H' '	Hexadecimal digit

Register Names

a	Address Variable
A	Accumulator
DC	Data Counter (Indirect Address Register)
DC_0	Data Counter #0 (Indirect Address Register #0)
DC_1	Data Counter #1 (Indirect Address Register #1)
DCL	Least significant 8 bits of Data Counter Addressed
DCU	Most significant 8 bits of Data Counter Addressed
H	Scratchpad Register #10 and #11
i and ii	immediate operand
ICB	Interrupt Control Bit
IS	Indirect Scratchpad Address Register
ISAR	Indirect Scratchpad Address Register
ISARL	Least Significant 3 bits of ISAR
ISARU	Most Significant 3 bits of ISAR
J	Scratchpad Register #9
K	Registers #12 and #13
KL	Register #13
KU	Register #12
PC_0	Program Counter
PC_0L	Least Significant 8 bits of Program Counter
PC_0U	Most Significant 8 bits of Program Counter
PC_1	Stack Register
PC_1L	Least Significant 8 bits of Program Counter
PC_1U	Most Significant 8 bits of Active Stack Register
Q	Registers #14 and #15
QL	Register #15
QU	Register #14
r	Scratchpad Register (any address thru 11)
W	Status Register

Scratchpad Addressing Modes (Machine Code Format)

r = C	(Hexadecimal), Register Addressed by ISAR (Unmodified)
r = D	(Hexadecimal), Register Addressed by ISAR; ISARL Incremented
r = E	(Hexadecimal). Register Addressed by ISAR; ISARL Decremented
r = F	(No operation performed)
r = 0 thru B	(Hexadecimal), Register 0 thru 11 addressed directly from the Instruction

Status Register

–	No change in condition
1/0	is set to "1" or "0" depending on conditions
CRY	Carry Flag
OVF	Overflow Flag
SIGN	Sign of Result Flag
ZERO	Zero Flag

POWER REQUIREMENTS: V_{DD} = +5.0 V ±5%; V_{GG} = +12.0 V ±5%; V_{SS} = 0 V; T_A = 0°C to 70°C; f = 2 MHz

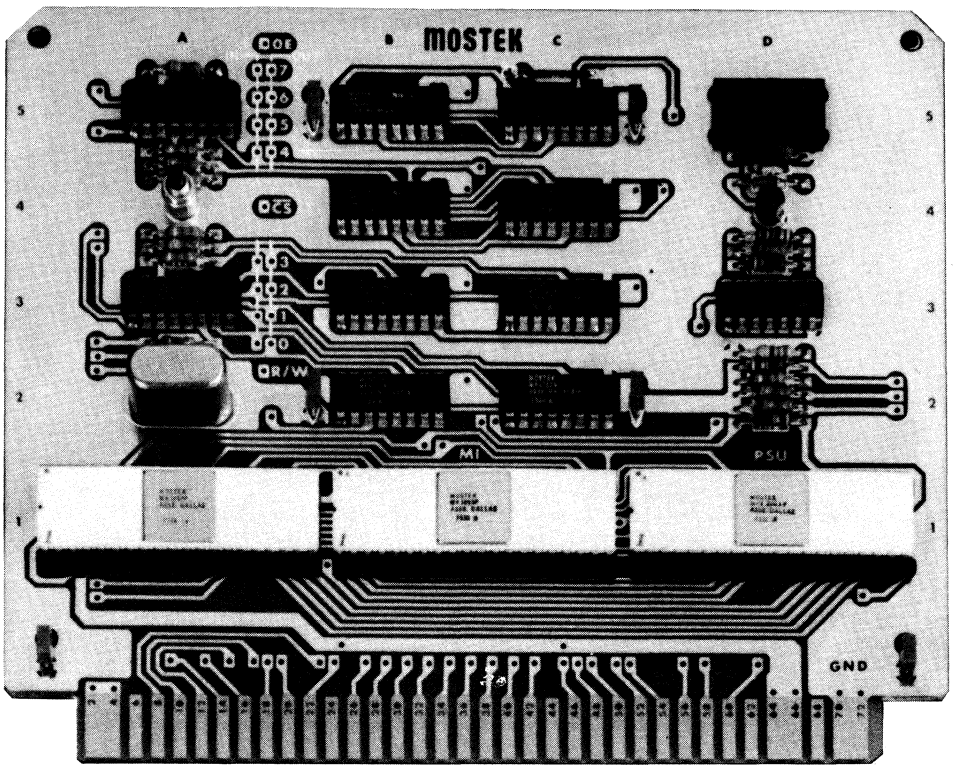
PART TYPE	SYMBOL	PARAMETER	TYP	MAX	UNITS	TEST CONDITIONS (Outputs Unloaded)
3850	I_{DD}	V_{DD} Current	30	80	mA	2 MHz
	I_{GG}	V_{GG} Current	15	25	mA	
3851	I_{DD}	V_{DD} Current	30	70	mA	2 MHz
	I_{GG}	V_{GG} Current	10	18	mA	
3852	I_{DD}	V_{DD} Current	35	70	mA	2 MHz
3853	I_{GG}	V_{GG} Current	13	30	mA	
3854	I_{DD}	V_{DD} Current	20	40	mA	2 MHz
	I_{GG}	V_{GG} Current	15	28	mA	

SIGNAL ELECTRICAL SPECIFICATIONS: V_{DD} = +5.0 V ±5%; V_{GG} = +12.0 V ±5%; V_{SS} = 0 V; T_A = 0°C to 70°C; f = 2 MHz

SIGNAL NAME (NUMBER, TYPE)	SOURCE OR RECEIVING DEVICE	V_{OH} MIN	V_{IH} MIN	V_{OL} MAX	V_{IL} MAX	LOAD
DATA BUS (8 INPUTS/OUTPUTS)	3850 3851 3852/3 3854	3.9	3.5	0.4	0.8	100 pF $I_{SOURCE} = -100\ \mu A$ $I_{SINK} = 900\ \mu A$
CONTROL BUS (5 OUTPUTS)	3850	3.9		0.4		100 pF, $I_{SINK} = 900\ \mu A$ $I_{SOURCE} = -100\ \mu A$
CONTROL BUS (5 INPUTS)[1]	3851 3852/3		3.5		0.8	
I/O PORTS (16 INPUTS/OUTPUTS)	3850 3851	2.9 (1 TTL) 3.9 (unloaded)	3.5[2]	0.4	0.8	100 pF plus 1 H-TTL Load
CLOCK REFERENCE (INPUT)	3850		4.0		0.8	
SYSTEM CLOCKS (PHI AND WRITE OUTPUTS)	3850	4.4		0.4		100 pF, $I_{SINK} = 900\ \mu A$ $I_{SOURCE} = -100\ \mu A$
SYSTEM CLOCKS (PHI AND WRITE INPUTS)	3851 3852/3 3854		4.0		0.8	
RESET (INPUT)	3850		3.5[2]		0.8	I_{IL} = 0.3 mA Max at $V_{IN} = V_{SS}$
INTERRUPT CONTROL BIT (OUTPUT)	3850	3.9		0.4		50 pF plus 100 μA I_{SOURCE} or I_{SINK}
INTERRUPT REQUEST (INPUT)	3850		3.5[2]		0.8	I_{IL} = 1 mA Max at V_{IN} = 0.4
INTERRUPT REQUEST (OUTPUT)	3851 3853	OPEN DRAIN		0.4		100 pF plus I_{SINK} = 1 mA
EXTERNAL INTERRUPT (INPUT)	3851 3853		3.5		1.2	
PRIORITY IN (INPUT)	3851 3853		3.5		0.8	
PRIORITY OUT (OUTPUT)	3851	3.9		0.4		50 pF plus 100 μA I_{SOURCE} or I_{SINK}
DBDR (OUTPUT)	3851	OPEN DRAIN[3]		0.4		100 pF plus I_{SINK} = 2.5 mA
ADDRESS LINES and RAM WRITE (16 OUTPUTS)	3852/3 3854	4.0		0.4		500 pF plus 2 TTL Loads
REGDR (INPUT/OUTPUT)	3852/3	3.9	3.5	0.4	0.8	100 pF plus 1 H-TTL Load
CPU READ (OUTPUT)	3852/3	3.9		0.4		50 pF plus 1 H-TTL Load
MEM IDLE, CYCLE REQ and CPU SLOT (OUTPUTS)	3852	3.9		0.4		50 pF plus 1 H-TTL Load
MEM IDLE (INPUT)	3854		3.5		0.8	
ENABLE, DIRECTION, TRANSFER, DMA WRITE SLOT, STROBE (OUTPUTS)	3854	3.9		0.4		50 pF plus 1 H-TTL Load
XFER REQ, P1,P2 (INPUTS)	3854		3.5		0.8	
LOAD REG, READ REG (INPUTS)	3854		3.5		0.8	

[1]3854 receives two control signals from external decoding device. [2]Internal pull-up resistor to V_{DD} [3]External pull-up resistor required.

F8 Evaluation Kit



INTRODUCTION

With the advent of MOSTEK's F8 Central Processing Unit (MK 3850) and the accompanying Program Storage Unit (MK 3851), the age of "Minimum Hardware Systems" has truly arrived. Many applications for which the cost of microprocessors could not be justified heretofore are being re-evaluated in light of the F8 CPU.

The designer will find that the 64 bytes of read/write memory internal to the CPU and the 1024 bytes of non-volatile PSU memory are sufficient for many application programs. TTL compatible latched input/output ports are present on both chips and allow the designer to forget about the extra circuitry needed to make system peripherals "look like a memory location". An internal programmable interrupting timer is available so that valuable CPU processing time is not taken up by software timing loops. A simple RC circuit will generate system timing when tolerance is not extremely critical or a crystal may be used.

As an initial aid toward evaluating the power and flexibility of the F8 system, MOSTEK offers the F8 Evaluation Kit described herein. This manual concerns itself with the description and subsequent use of the kit which upon completion requires only a Teletype-like terminal and +5/+12 VDC power supplies. Immediate system intelligence is given by a firmware program residing in the PSU called the Designers Development Tool 1 or DDT-1. This program is described within and may be used in conjunction with the 1024 bytes of MK 4102 RAM memory to develop application programs for possible installation into a PSU later.

A sample user program is also provided to acquaint the designer with the F8 machine language. The program is discussed in detail from inception to execution thus allowing even the most inexperienced user to program the completed F8 Kit.

F8 EVALUATION KIT DESCRIPTION

As shown in Figure 1 the F8 Evaluation Kit is composed of the following:

CPU - Central Processing Unit
PSU - Program Storage Unit
SMI - Static Memory Interface
RAM - 1024 bytes of static RAM
Teletype interface

This configuration provides the user with a system having these features:

6.75 in. x 5.50 in. Printed Circuit Board
24 bits of I/O ports available to user
1024 bytes RAM
Full duplex TTY interface (20mA loop)
Crystal controlled clock
Non-volatile operating system in PSU

FUNCTIONAL BLOCK DIAGRAM

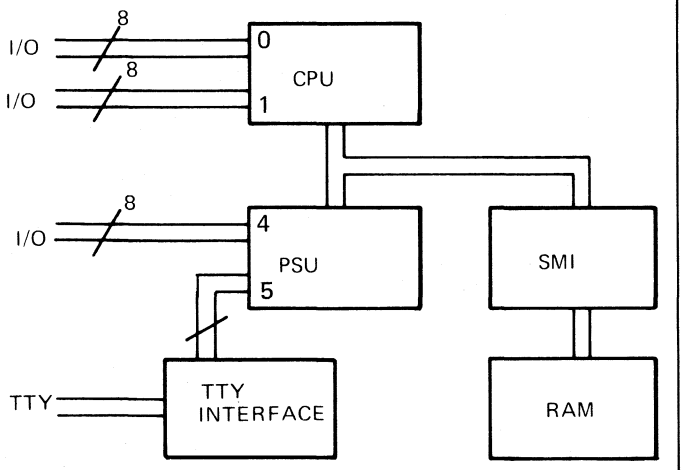
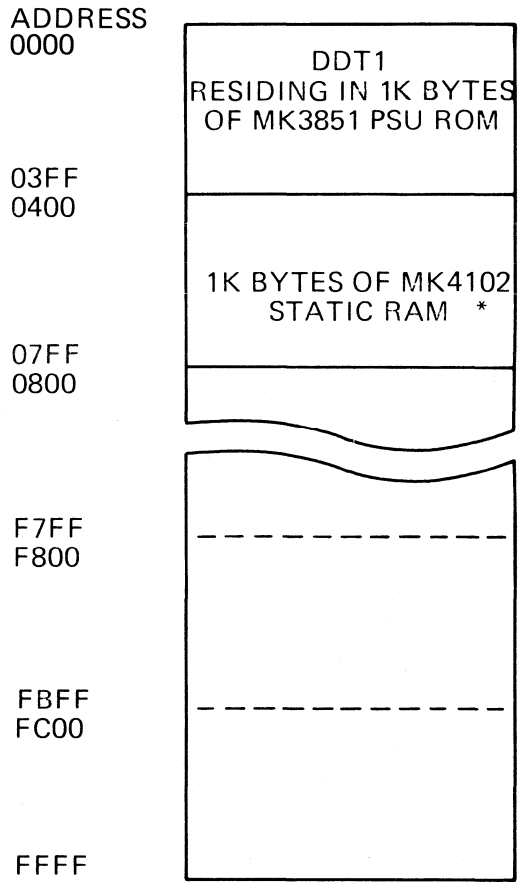


Figure 1

The MK 3853 Static Memory Interface (SMI) integrated circuit provides the necessary address and write signals for the 1K x 8 bit static RAM memory which is constructed with eight MK 4102 1K bit static RAMs.

MEMORY MAP



* The 1K of RAM can be addressed at all 1K intervals up to address FFFF.

Figure 2

The Designers Development Tool 1 (DDT-1) program resides in the Program Storage Unit (PSU) which is located in the low order 1K bytes of the memory space. Refer to the memory map in Figure 2. Partial decoding of the RAM address causes the 1024 bytes of static RAM to effectively exist in the second 1K bytes of memory as well as in each of the subsequent 1K bytes of memory.

Figure 3 (on pages 92 & 93) is a schematic of the F8 Evaluation Kit circuitry. The Basic clock oscillator and clock generation circuitry is contained in the CPU integrated circuit. A 2 MHz crystal determines the clock frequency for the CPU.

As shown in Figure 4 which describes the F8 Kit port assignments, Port 0, Port 1, and Port 4 are available at the edge connector. Port 0 and Port 1 are CPU I/O ports. Port 4 and Port 5 are PSU I/O ports.

All eight bits of Port 0, Port 1, and Port 4 are available to the user.

The high order four bits of Port 5 are allocated for the full duplex Teletype interface circuitry. Bit 4 of

Port 5 selects a 110 baud Teletype rate when not connected. This bit (Pin 45 on the edge connector) may be connected to ground to select a 300 baud rate. When operating at the 110 baud rate, an eleven bit TTY format is used (two stop bits). When operating at the 300 baud rate, a ten bit TTY format is used (one stop bit). Bit 5 of Port 5 is used to drive an external Teletype punched tape reader step circuit in order to read a single frame of punched tape at a time. Bit 6 of Port 5 is the Teletype printer data output. Approximately a 20mA current loop is established by the +12 VDC power supply and the 680 Ohm current limiting resistor in series with the TTL 7406 printer

F8 KIT PORT ASSIGNMENTS

Port 0

B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0

(available to user)

Port 1

B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0

(available to user)

Port 4

B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0

(available to user)

Port 5

B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0

TTY I/O

Bit 4 Baud Rate Select
floating = 110
grounded = 300

Bit 5 Relay Step Signal
advance = 1
normal = 0

Bit 6 Terminal Data Out
mark = 1
space = 0

Bit 7 Terminal Data In
mark = 1
space = 0

Figure 4

driver. Bit 7 of Port 5 is the Teletype keyboard serial input port. A transistor interface circuit provides signal conditioning for the Teletype keyboard signal.

Connections to the Teletype are made using a sixteen pin integrated circuit socket on the evaluation board. This socket, located in the upper right corner of the printed circuit board, is illustrated in Figure 5 showing the pins designated for Teletype connections.

F8 KIT TELETYPE CONNECTOR

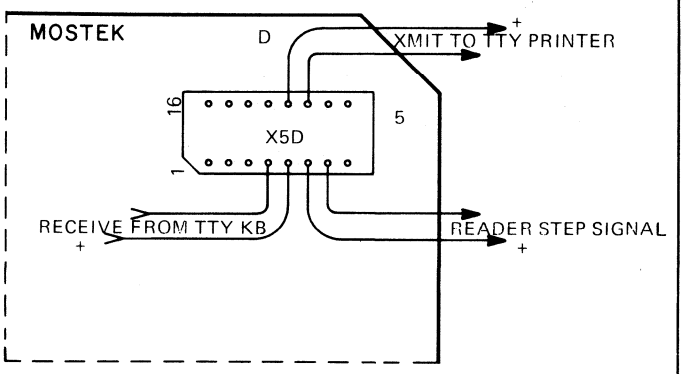


Figure 5

Pins four and five of this socket form the current loop from the TTY keyboard. Pins six and seven drive the tape reader external step circuitry. Pins eleven and twelve drive the TTY printer. Note polarity markings on pins 5,6 and 12 in Figure 5.

Power requirements for the F8 Evaluation Kit board are given below.

POWER REQUIREMENTS

VOLTAGE	CURRENT
+12 VDC ± 5%	120mA
+5 VDC ± 5%	750mA

The following table lists each pin of the edge connector and the signal present at that pin.

PCB EDGE CONNECTOR PIN ALLOCATION TABLE

Pin Number	Signal Name	Pin Number	Signal Name
1	+5 VDC	2	+5 VDC
3	+5 VDC	4	+5 VDC
5	NO CONNECTION	6	NO CONNECTION
7	PORT 1 BIT 0	8	PORT 0 BIT 0
9	PORT 1 BIT 1	10	PORT 0 BIT 1
11	PORT 1 BIT 2	12	PORT 0 BIT 2
13	PORT 1 BIT 3	14	PORT 0 BIT 3
15	PORT 1 BIT 4	16	PORT 0 BIT 4
17	PORT 1 BIT 5	18	PORT 0 BIT 5
19	PORT 1 BIT 6	20	PORT 0 BIT 6
21	PORT 1 BIT 7	22	PORT 0 BIT 7
23	NO CONNECTION	24	NO CONNECTION
25	NO CONNECTION	26	EXTERNAL INTERRUPT
27	ADDRESS BIT 15	28	ADDRESS BIT 7
29	ADDRESS BIT 14	30	ADDRESS BIT 6
31	ADDRESS BIT 13	32	ADDRESS BIT 5
33	ADDRESS BIT 12	34	ADDRESS BIT 4
35	ADDRESS BIT 11	36	ADDRESS BIT 3
37	ADDRESS BIT 10	38	ADDRESS BIT 2
39	ADDRESS BIT 9	40	ADDRESS BIT 1
41	ADDRESS BIT 8	42	ADDRESS BIT 0
43	NO CONNECTION	44	NO CONNECTION
45*	PORT 5 BIT 4	46	PORT 4 BIT 7
47	PORT 5 BIT 3	48	PORT 4 BIT 6
49	PORT 5 BIT 2	50	PORT 4 BIT 5
51	PORT 5 BIT 1	52	PORT 4 BIT 4
53	PORT 5 BIT 0	54	PORT 4 BIT 3
55	NO CONNECTION	56	PORT 4 BIT 2
57	TTY TAPE READER STEP (+)	58	PORT 4 BIT 1
59	TTY KEYBOARD (–)	60	PORT 4 BIT 0
61	TTY PRINTER (–)	62	NO CONNECTION
63	+12 VDC	64	+12 VDC
65	+12 VDC	66	+12 VDC
67	NO CONNECTION	68	NO CONNECTION
69	GND	70	GND
71	GND	72	GND

* Pin 45 should be connected to ground (GND) for 300 baud operation. Pin 45 should not be connected for 110 baud operation.

TTY SOCKET PIN ALLOCATION TABLE

Pin Number	Signal Name
4	TTY Keyboard (–)
5	TTY Keyboard (+)
6	TTY Reader Step (+)
7	TTY Reader Step (–)
11	TTY Printer (–)
12	TTY Printer (+)

DDT-1

The Designers Development Tool 1 (DDT-1) is a 1024 byte program residing in the non-volatile MK 3851 Program Storage Unit which provides the user with a completely self-contained operating system for the F8 Kit. Full duplex, selectable 110 or 300 baud rate I/O drivers within DDT-1 enable the user to communicate with the microprocessor using a Teletype or CRT terminal. The program serves as convenient means for evaluating the F8 and the debugging of application programs. A summary of the commands accepted by DDT-1 is as follows:

- B - Breakpoint (software) address
- C - Copy memory arrays
- D - Dump memory onto paper tape
- E - Execute at specified address
- H - Hexadecimal arithmetic operations
- L - Load memory from paper tape
- M - Memory content display and modify
- P - Port content display and modify
- T - Type memory content array

Several operational characteristics of DDT-1 should be noted by the user prior to exercising the program. The command request mode prints a period (.) upon RESET and awaits the keyin of a B,C,D,E,H,L,M,P, or T character. Correct response to a command is verified when the keyed character is printed followed by a space. Illegal command characters are also printed but the hexadecimal arithmetic (H) mode is entered through default. Depending upon the command, up to three numeric operand fields may be required. Each operand field is composed of one to four hexadecimal digits and is terminated by a comma except the last which ends with a carriage return. A numeric keyin error during an operand field entry may be corrected by re-keying the value as four digits to completely clear the erroneous number. A period (.) entered in the operand field causes DDT-1 to abort the current command and to await the next request.

BREAKPOINT

Breakpoint (control trap) address may be set to cause user program execution to halt at a specified location in the program and return control to DDT-1 for register and/or memory inspection.

FORMAT: B aaaa

PROCEDURE:

1. Enter the character B from the keyboard.
2. Enter the address (aaaa) of the first byte of instruction at which control is to be intercepted in the user program.
3. Enter a carriage return (CR).

```
LR      QL,A
JMP     H'0005'
```

   The above trap instruction sequence is then placed in the user's program beginning at the previously specified address (aaaa).

4. Enter user program execution address as described in the EXECUTE command section.
5. A period (.) indicates control successfully encountered the breakpoint and the command mode has resumed.
6. Working registers and/or memory may be inspected using the TYPE or MEMORY commands. Refer to the BREAKPOINT MEMORY DISPLAY MAP for the location of the desired register values.

NOTE:

a. The four bytes of user code replaced by the trap instruction sequence are saved at command time and then restored when the breakpoint address is encountered by control.

b. All registers and status except Register Q are preserved in the last available eighty bytes of RAM.

c. The EXECUTE command always copies the RAM save area back into the appropriate registers.

BREAKPOINT MEMORY DISPLAY MAP

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
FFB –	XX	H'2A'	DC_{up}	DC_{lo}	H'0D'	BPA_{up}	BPA_{lo}	UC_1	UC_2	UC_3	UC_4	$PC1_{up}$	$PC1_{lo}$	W	ACC	ISAR
FFC –	r0	r1	r2	r3	r4	r5	r6	r7	r8	(J) r9	(H) rA	rB	(K) rC	rD	DC_{up}	DC_{lo}
FFD –	r10	r11	r12	r13	r14	r15	r16	r17	r18	r19	r1A	r1B	r1C	r1D	r1E	r1F
FFE –	r20	r21	r22	r23	r24	r25	r26	r27	r28	r29	r2A	r2B	r2C	r2D	r2E	r2F
FFF –	r30	r31	r32	r33	r34	r35	r36	r37	r38	r39	r3A	r3B	r3C	r3D	r3E	r3F

Note:
- FFB0 unused by DDT-1.
- FFB1 - FFB4 user program's re-entry sequence set up by EXECUTE command.
- FFB5 - FFB6 current BREAKPOINT ADDRESS requested by user.
- FFB7 - FFBA USER CODE replaced by the BREAKPOINT sequence.
- FFBB - FFBC contents of PC1 at the time of BREAKPOINT.
- FFBD contents of Status Register W at the time of BREAKPOINT.
- FFBE contents of Accumulator (ACC) at the time of BREAKPOINT.
- FFBF contents of Indirect Scratchpad Address Register (ISAR) at BREAKPOINT.
- FFC0 - FFFF contents of Scratchpad Registers r0 through r3F except Register Q (rE, rF).
- FFCE - FFCF contents of Data Counter (DC) as received by an LR Q,DC instruction at the time of BREAKPOINT thereby making Register Q volatile.

COPY

The contents of a block of memory may be copied into another area of memory beginning at a start address specified in the command format.

FORMAT: C ssss,ffff,dddd

PROCEDURE:

1. Enter the character C from the keyboard.
2. Enter the start address (ssss) and the finish address (ffff) of the block of memory that is to be copied into the new location. Enter the destination address (dddd) of the first byte of the block of memory data.
3. Enter a carriage return (CR) for the copy process to begin. The command mode then resumes.

DUMP

The contents of memory may be punched onto paper tape in the printable F8 assembler format.

FORMAT: D ssss,ffff

PROCEDURE:

1. Enter the character D from the keyboard.
2. Enter the start address (ssss) and the finish address (ffff) of the memory block to be dumped in the assembler format.
3. Place the tape punch switch in the ON position.
4. Enter a carriage return (CR) from the Teletype keyboard.
5. Dump process may be terminated by pressing the RESET push button.

EXECUTE

The starting location of program execution may be specified anywhere within the range of the available memory.

FORMAT: E ssss

PROCEDURE:

1. Enter the character E from the keyboard.
2. Enter the start address (ssss) in the format shown above.
3. Enter a carriage return (CR). Execution begins immediately at the specified address.

NOTE:

a. The EXECUTE command always copies the RAM save area back into the appropriate registers.

b. The Interrupt Control Bit (ICB) is set by bit 4 of byte FFBD.

HEXADECIMAL ARITHMETIC

The arithmetic routine will calculate the sums and differences of hexadecimal numbers that are less then 16 bits in size. All input and output number sequences are truncated to two eight bit bytes (i.e. 2E1C3 +0= E1C3).

FORMAT: H a+b = result

or

H aaaa+bbbb-cccc = result

PROCEDURE:

1. Enter the character H from the keyboard.
2. Enter the expression to be evaluated. This expression may be composed of single hexadecimal characters or groups of hexadecimal characters as shown in the format above.
3. Enter equal (=) to produce current result.
4. Enter comma (,) to clear result register and start new calculation.
5. Enter carriage return (CR) and command mode resumes.

LOAD

Paper tapes punched in F8 assembler output format may be loaded from the reader.

PROCEDURE:

1. Place the tape reader switch in the STOP position.
2. Place the leader of the new tape into the tape reader.
3. Enter the character L from the keyboard and place the tape reader switch in the START position.

NOTE:

a. Teletypes that are equipped with automatic read circuitry will stop at the end of the load and return to the command input mode. However, those Teletypes not so equipped will continue to read tape data as command directives.

b. Data from the tape will be loaded into memory starting at the load address contained in the first four frames of the tape after the frame containing the start character (S).

c. During a tape load the address of any checksum errors will be printed at the end of each eight bytes. This is an indication that any of the previous eight bytes of data may be incorrect however, loading continues.

MEMORY

The contents of any memory location may be examined and modified by the MEMORY command.

FORMAT: M aaaa

PROCEDURE:

1. Enter the character M from keyboard.
2. Enter the address of the memory location that is to be examined in the format shown above. The address (aaaa) will be printed along with the contents of that location.
3. In order to examine the next byte of memory enter a carriage return (CR).
4. In order to examine preceeding bytes of memory enter an up caret (^) character.
5. In order to modify the contents of a memory location enter the value to be placed into that location followed by a carriage return (CR).
6. Upon completion of the memory examine and modify procedures, enter a period (.) to return to the command input mode.

NOTE:

a. In place of the address (aaaa) in the operand field, an R keyin is a symbolic representation of the memory address FFC0 which is the first location of the Scratchpad Register Save Area. Hexadecimal expressions may be used with R. As an example scratchpad Register 3F may be addressed as R + 3F.

b. In place of the address (aaaa) in the operand field, an asterisk (*) keyin is a symbolic representation of the address currently in data counter. The displayed memory value is the one addressed by the data counter. Hexadecimal expressions may be used with the asterisk.

PORT

Allows the input/output ports to be examined and modified.

FORMAT: P pp

PROCEDURE:

1. Enter the character P from the keyboard.
2. Enter the number (pp) of the port to be examined.
3. Enter a carriage return (CR). The port selected along with the data on that port will be displayed.
4. In order to modify the contents of a port enter the value to be placed in the port followed by a carriage return.
5. After completion of the port examine and modify procedure enter a period (.) to return to the command input mode.

TYPE

The contents of a block of memory can be printed by using the TYPE command. The print format consists of a four character hexadecimal address followed by 16 eight-bit bytes of data on each line. The address printed is the address of the first byte of data on that line.

FORMAT: T ssss,ffff

PROCEDURE:

1. Enter the character T from the keyboard.
2. Enter the start address (ssss) and the finish (ffff) address of the memory block to be printed.
3. Enter a carriage return on the keyboard.

NOTE:

a. See MEMORY command NOTE.

F8 EVALUATION KIT PROGRAMMING EXAMPLE

Once the F8 kit has been assembled many users are faced with the unfamiliar task of programming a microprocessor. Generally a simple, well explained program example is sufficient means for providing the designer with an introduction to the programming process.

A program is a set of instructions to a computer causing it to process data and produce specific results as desired by the user. In fact the MK 3851 Program Storage Unit contains a program called Designers Development Tool 1 (DDT-1). Portions of this program are used in the sample program discussed in the following text.

A first step in the programming process is to define the task or determine the purpose of the program to be written. The goal in the sample program is to cause the Teletype or terminal device to behave as a typewriter until a period (.) is entered. Upon encountering a period computer control will return to DDT-1.

A second step in the process involves a flowchart or a verbal/pictorial method for representing the flow of logic necessary for the program to function properly. The flowchart in Figure 6 represents the following logic statements for implementing the program.

1. Initialize DDT-1 input/output program registers,
2. Enter a character using the keyboard driver in DDT-1,
3. Compare this character to a period,
4. If equal return to DDT-1 (at which time a carriage return, line feed and period are sent to the terminal device).
5. Otherwise, echo or print the keyed character using the printer driver in DDT-1,
6. Branch to statement 2 above.

An assembler is a program designed to read (source) statements consisting of characters representing a computer instruction and convert them to the appropriate numerical machine (object) codes necessary to be understood by a computer. Page 12 contains the F8 Sample Program Assembly which serves as a guide during the discussion of the program.

FLOWCHART

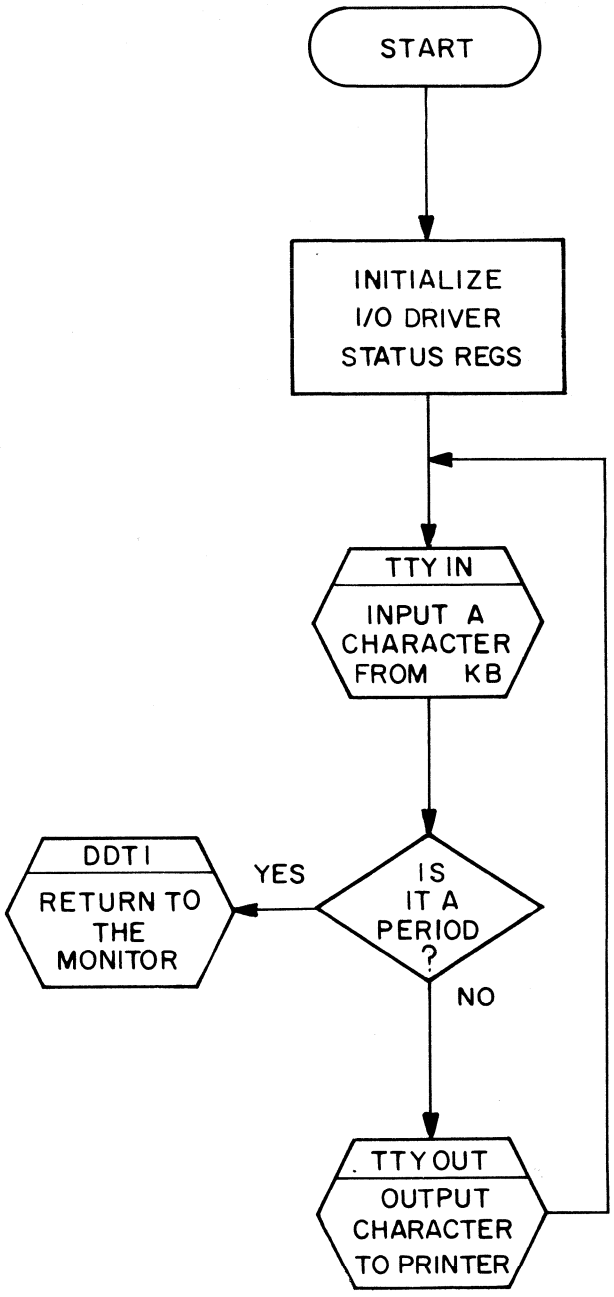


Figure 6

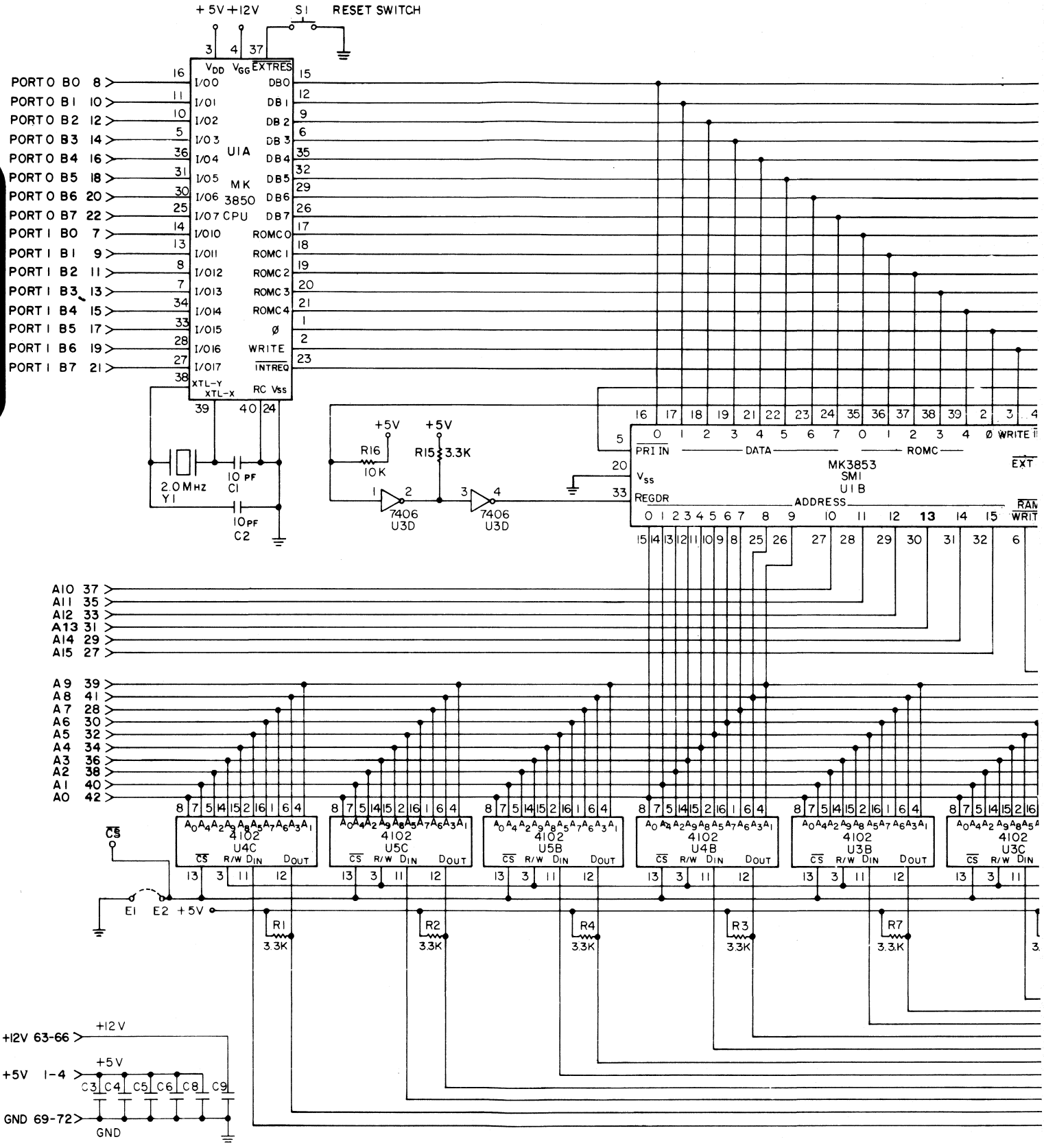
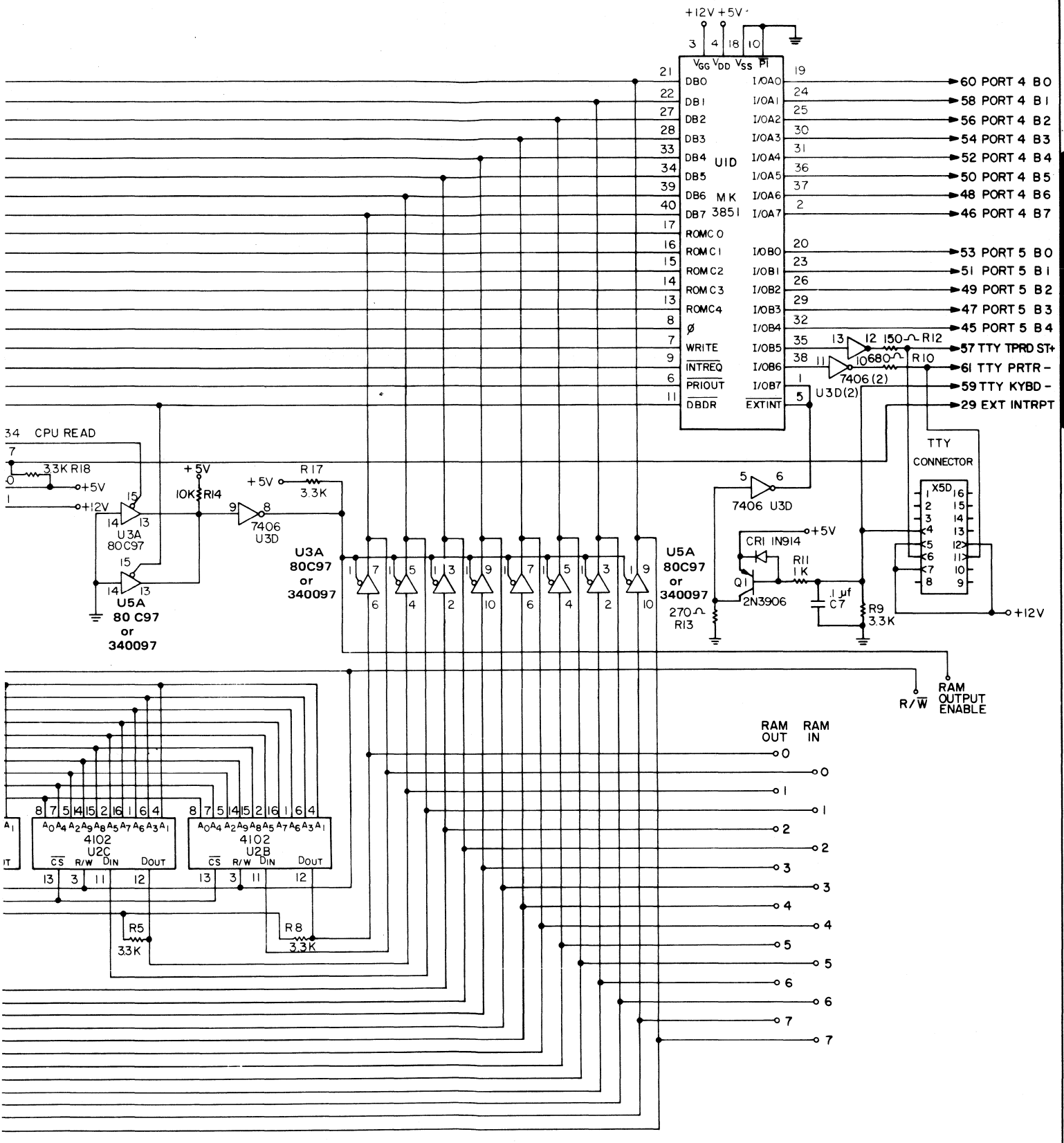

+5V +12V
S1 RESET SWITCH
MK 3850 CPU
U1A
PORT 0 B0 8
PORT 0 B1 10
PORT 0 B2 12
PORT 0 B3 14
PORT 0 B4 16
PORT 0 B5 18
PORT 0 B6 20
PORT 0 B7 22
PORT 1 B0 7
PORT 1 B1 9
PORT 1 B2 11
PORT 1 B3 13
PORT 1 B4 15
PORT 1 B5 17
PORT 1 B6 19
PORT 1 B7 21
2.0 MHz Y1
10 PF C1
10PF C2
R16 10K
R15 3.3K
7406 U3D
MK3853 SMI U1B
A10 37
A11 35
A12 33
A13 31
A14 29
A15 27
A9 39
A8 41
A7 28
A6 30
A5 32
A4 34
A3 36
A2 38
A1 40
A0 42
4102 U4C
4102 U5C
4102 U5B
4102 U4B
4102 U3B
4102 U3C
E1 E2 +5V
R1 3.3K
R2 3.3K
R4 3.3K
R3 3.3K
R7 3.3K
+12V 63-66
+5V 1-4
GND 69-72
C3 C4 C5 C6 C8 C9

Figure 3


+12V +5V
3 4 18 10
VGG VDD VSS PI
UID MK 3851
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
ROMC0
ROMC1
ROMC2
ROMC3
ROMC4
Ø
WRITE
INTREQ
PRIOUT
DBDR
I/OA0
I/OA1
I/OA2
I/OA3
I/OA4
I/OA5
I/OA6
I/OA7
I/OB0
I/OB1
I/OB2
I/OB3
I/OB4
I/OB5
I/OB6
I/OB7
EXTINT
60 PORT 4 B0
58 PORT 4 B1
56 PORT 4 B2
54 PORT 4 B3
52 PORT 4 B4
50 PORT 4 B5
48 PORT 4 B6
46 PORT 4 B7
53 PORT 5 B0
51 PORT 5 B1
49 PORT 5 B2
47 PORT 5 B3
45 PORT 5 B4
57 TTY TPRD ST+
61 TTY PRTR –
59 TTY KYBD –
29 EXT INTRPT
R12 150Ω
R10 680Ω
7406 (2)
U3D(2)
34 CPU READ
3.3K R18
+5V
+12V
10K R14
U3A 80C97
U5A 80 C97 or 340097
R17 3.3K
7406 U3D
U3A 80C97 or 340097
U5A 80C97 or 340097
270Ω R13
7406 U3D
CR1 IN914
R11 1K
Q1 2N3906
1 µf C7
R9 3.3K
TTY CONNECTOR
X5D
+12V
R/W
RAM OUTPUT ENABLE
RAM OUT
RAM IN
4102 U2C
4102 U2B
CS R/W DIN DOUT
R5 3.3K
R8 3.3K

F8 SAMPLE PROGRAM ASSEMBLY

MEMORY LOC	MACHINE CODE	STATEMENT NOS.	SOURCE STATEMENTS			COMMENTS
		1		ORG	H'0500'	ORIGIN OF PROGRAM IN F8 RAM MEMORY
		2	TTYIN	EQU	H'03F3'	PSU ADDRESS OF TELETYPE INPUT ROUTINE
		3	TTYOUT	EQU	H'035D'	PSU ADDRESS OF TELETYPE OUTPUT ROUTINE
		4	DDT1	EQU	H'0000'	PSU ADDRESS FOR RETURN TO DDT-1
			*			
			*			
500	20	5	START	LI	H'FF'	ACCUMULATOR IS LOADED WITH HEX FF (8 BITS)
501	FF					
502	0B	6		LR	IS,A	USE TO INITIALIZE ISAR TO HEX 3F (6 BITS)
503	54	7		LR	4,A	USE TO INITIALIZE INPUT STATUS REG TO
504	34	8		DS	4	HEX FE FOR 'NO INPUT CHARACTER READY'
505	56	9		LR	6,A	USE TO INITIALIZE OUTPUT STATUS REG TO
			*			HEX FF FOR 'CHARACTER OUTPUT FINISHED'
506	71	10		LIS	H'1'	ACCUMULATOR LOADED WITH CODE HEX 01
507	B6	11		OUTS	6	OUTPUT TO TIMER PORT TO ENABLE EXT INTERRUPT
508	1B	12		EI		ENABLE CPU TO BE INTERRUPTED BY I/O DRIVERS
			*			
			*			
509	28	13	LOOP	PI	TTYIN	CALL INPUT ROUTINE IN DDT-1 AT THE HEX
50A	03					ADDRESS 03F3 WITH THE SEVEN BIT ASCII
50B	F3					CODE FOR THE CHARACTER RETURNED VIA R-S
50C	4C	14		LR	A,S	COPY CHARACTER CODE INTO ACCUMULATOR
50D	25	15		CI	C'.'	COMPARE CHARACTER IN THE ACCUMULATOR WITH
50E	2E					THE ASCII CODE FOR A PERIOD
50F	94	16	HERE1	BNZ	ECHO	BRANCH IF COMPARISON FALSE
510	04					
511	29	17		JMP	DDT1	YES, RETURN TO DDT-1 MONITOR WHICH PRINTS
512	00					A CARRIAGE RETURN, LINE FEED FOLLOWED
513	00					BY A PERIOD AND AWAITS NEXT COMMAND
			*			
514	28	18	ECHO	PI	TTYOUT	REMEMBER THAT REG S MUST CONTAIN OUTPUT CODE.
515	03					CALL OUTPUT ROUTINE IN DDT-1 AT THE HEX
516	5D					ADDRESS 035D WITH THE SEVEN-BIT ASCII
517	90	19	HERE2	BR	LOOP	CODE FOR THE CHARACTER IN REG S
518	F1					MAINTAIN EXECUTION LOOP
		20		END		MARKS END OF SOURCE STATEMENTS TO ASSEMBLER
						NOTE: REG S IS REGISTER ADDRESSED BY ISAR (IS)

Each sample program source statement appears below in capital letters with an explanation immediately following.

ORG H'0500'

Statement 1 is an assembler directive to begin this program's object code generation at hexadecimal memory location 0500. Machine code is not created by this statement but note that the code for the first F8 instruction (statement 5) does begin at the address thus specified.

TTYIN EQU H'03F3'

Statement 2 is used to inform the assembler as to the hexadecimal memory address (03F3) of the character input program residing in DDT-1. No machine code is generated.

TTYOUT EQU H'035D'

Statement 3 is used to inform the assembler as to the hexadecimal memory address (035D) of the character output program residing in DDT-1. No machine code is generated.

DDT1 EQU H'0000'

Statement 4 is used to inform the assembler as to the hexadecimal memory address (0000) of the DDT-1 monitor program. No machine code is generated.

START LI H'FF'

Statement 5 begins with a label symbol called START which is used by the assembler to mark hexadecimal (hex) address 0500 or the start of this program in F8 read/write memory. The operation (op code) field contains the Load Immediate (LI) instruction mnemonic which is interpreted by the F8 assembler as machine code hex 20 to be placed in memory at location 0500. The operand field contains H'FF' representing the hex number FF to be placed in memory at location 0501. Note that it is immediately after the hex 20 machine code. When this instruction is executed, the F8 accumulator (A) will have all eight bits set to one.

LR IS,A

Statement 6 contains the Load Register (LR) op code and operand IS,A which is translated by the assembler into machine code hex 0B to be placed in memory at location 0502. This instruction copies the low order six bits of the accumulator (A) into the Indirect Scratchpaid Address Register (ISAR) designated here as IS. The contents of the accumulator are not altered. ISAR is a six bit register which will address

any of the 64 eight bit registers in the CPU. The purpose of this instruction is to insure that ISAR addresses a register other than Register 4 through Register 9. These registers are used by the input/output (I/O) routines in DDT-1. Upon execution of this instruction, ISAR will contain the maximum value of hex 3F so that the character received and transmitted in this program is via Register 3F. Any register currently addressed by ISAR shall be called Reg S.

```
LR      4,A
```

Statement 7 contains another Load Register (LR) op code and an operand of 4,A which translates into machine code hex 54 to be installed in memory at location 0503. This instruction will copy all the accumulator (A) bits into Scratchpad Register 4. Note that this register was directly addressed thus eliminating the need for addressing indirectly through ISAR. The value of hex 3F in ISAR is maintained and the accumulator is unaltered.

```
DS      4
```

Statement 8 contains the Decrement Scratchpad (DS) op code and the operand 4 which is converted to machine code hex 34 to be placed in memory location 0504. This instruction's function is to decrement or subtract one from the value in Register 4 so that it's contents will be hex FE. Register 4 is used to initialize the input program in DDT-1 to 'no input character ready' in order to start the sample program's input operation in a stable state.

```
LR      6,A
```

Statement 9 contains a Load Register (LR) op code and the operand 6,A translated by the assembler into machine code hex 56 to be placed into location 0505. This instruction copies all the accumulator (A) bits into Scratchpad Register 6 loading it with hex FF. The accumulator value is unaltered. Register 6 is used to initialize the output program in DDT-1 to 'character output finished' in order to start the sample program's output operation in a stable state.

```
LIS     H'1'
```

Statement 10 contains a Load Immediate Short (LIS) op code and operand H'1' translated into machine code hex 71. The immediate data value of 1 is contained in the low order four bits of the same instruction byte. The machine code is placed at location 0506. When this instruction is executed the four high order bits of the accumulator are zeroed and the low order four bits contain the immediate data value of one. Note the difference between this instruction and the statement 5 instruction.

```
OUTS    6
```

Statement 11 contains the Output to Port (OUTS) op code and the port number 6 in the operand field. The assembler translates this statement into machine code hex B6 to be placed at memory location 0507. Note that the second digit of the generated code reflects the port number. This instruction outputs the eight bit contents (hex 01) of the accumulator to the timer port in order to enable external interrupts for the I/O programs in DDT-1.

```
EI
```

Statement 12 contains the Enable Interrupts (EI) op code only. It is translated into machine code hex 1B and resides at location 0508. This instruction enables local interrupts to the CPU so that the I/O programs in DDT-1 can function.

```
LOOP    PI      TTYIN
```

Statement 13 begins with a label symbol called LOOP which is used by the assembler to mark hexadecimal address 0509. The operation field contains the Push Immediate (PI) instruction op code and causes the F8 assembler to generate hex machine code 28 to be placed at memory location 0509. This instruction forces computer control to branch to the instruction at the memory location (03F3) represented by TTYIN, but to remember the next instruction to be executed upon returning is at 050C. This CPU action is termed a 'subroutine call' and is useful in utilizing instruction sequences that are common to other programs. The subroutine call demonstrated here requests a character from the input device and returns with the 7-bit ASCII character code in Register S. Register S denotes Scratchpad Register 3F as currently addressed by ISAR.

```
LR      A,S
```

Statement 14 contains an instruction that copies the ASCII character code in S (Register 3F) into the accumulator. This must be done since comparisons cannot be made without using the accumulator. Hex code 4C is placed at location 050C. Note that the second digit in the generate code is hex C which causes the register addressed by ISAR to be used during the execution of this instruction.

```
CI      C'.'
```

Statement 15 contains the Compare Immediate (CI) op code which translates into machine code hex 25 to be installed at 050D. The operand C'.' causes the assembler to supply the equivalent ASCII code for the period character enclosed in primes. The hex value (2E) is to be placed in the location immediately following 050D. The purpose of the instruction is to compare the 7 bit ASCII character code now in the accumulator with that of a period. The zero flag bit in the Status Register W (refer to programming manual) is set to one for true comparisons and zero for false comparisons. The accumulator value is unaltered.

HERE1 BNZ ECHO

Statement 16 contains an instruction which tests the previously mentioned Status Register W and causes computer control to branch to the memory location labelled ECHO (hex 0514) if the above comparison was false. A true condition (period was entered) causes control to execute the JMP DDT1 instruction. The assembler generates a machine code hex 94 for the Branch Not Zero (BNZ) op code. This value is placed at memory location 050F. The next address contains the number of memory bytes that control must branch over in order to reach the address (0514) represented by ECHO. This value must not exceed hex 7F for forward branches. The displacement byte count is computed in the following manner.

[(ECHO - HERE1) - 1]
or
(0514 - 050F) - 1 = 4

This hex value 04 is to be placed in the next memory location 0510.

JMP DDT1

Statement 17 contains the Jump (JMP) op code which the assembler translates into machine code hex 29 to be placed at location 0511. The operand DDT1 represents the sixteen bit address for the start of the Designers Development Tool 1 program in PSU memory. This hexadecimal address is placed in the next two memory locations with the most significant byte at 0512 and the least significant byte at 0513. Note that a sixteen bit address will allow computer control to jump to any address in the 65K memory range. Since the accumulator is used in the jump operation, its value is destroyed. As previously stated this instruction is executed when a period is entered.

ECHO PI TTYOUT

Statement 18 contains a subroutine call to the output instruction residing in the DDT-1 program. Remember that Reg S must address the byte of ASCII code to be printed.

HERE2 BR LOOP

Statement 19 contains an instruction which causes an unconditional branch back to the subroutine call for character entry through the keyboard. The Branch Relative (BR) op code translates into machine code hex 90 to be placed at location 0517. The operand LOOP represents address 0509 which is backward reference relative to the current instruction address of 0517. The next byte of this instruction contains the negative (high bit on) number of memory bytes that must be branched over in order to reach the address 0509. This value must not exceed hex FF for backward branches. The negative displacement byte count is computed in the following manner.

[FF - (HERE2 - LOOP)]
or
FF - (0517 - 0509) = F1

The hex value F1 is to be placed in the next memory location 0518.

END

Statement 19 is an assembler directive that all statements to be assembled have been read in.

Now that the specific instructions have been discussed, the user should install or load the program into F8 memory for execution. The Designers Development Tool 1 (DDT-1) provides a convenient means for accomplishing the load. The following page is actual output from DDT-1 illustrating:

1. installation of program into memory
2. verifying program load
3. executing the program
4. dumping the program onto paper tape
5. loading the program from the tape
6. executing with a breakpoint
7. inspecting registers
8. port inspection

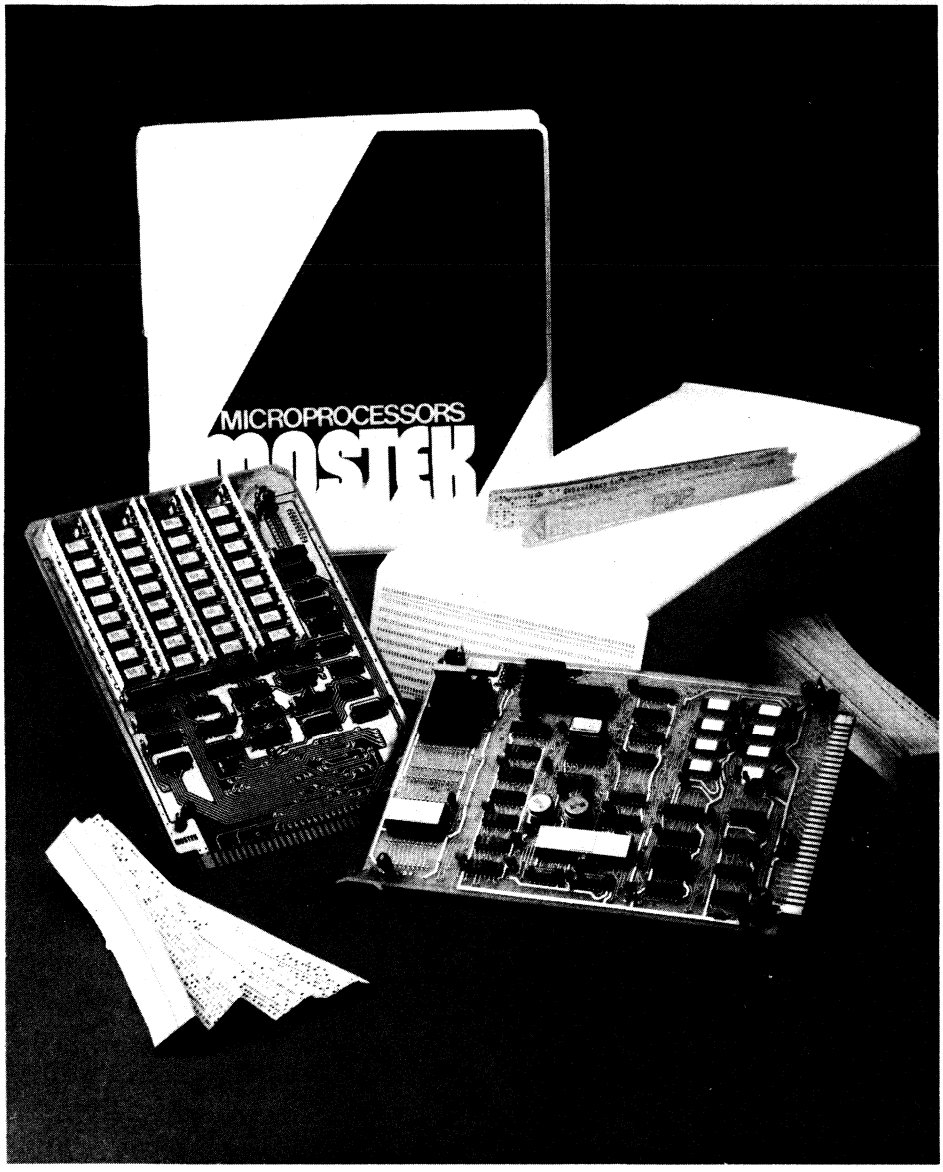
```
.M 500
0500 00 20
0501 00 FF
0502 00 0B
0503 00 54
0504 00 34
0505 00 56
0506 00 71
0507 00 B6
0508 00 1B
0509 00 28
050A 00 03
050B 00 F3
050C 00 4C
050D 00 25
050E 00 2E
050F 00 94
0510 00 04
0511 00 29
0512 00
0513 00
0514 00 28
0515 00 03
0516 00 5D
0517 00 90
0518 00 F1
0519 00 .
.T 500,518
0500  20 FF 0B 54  34 56 71 B6  1B 28 03 F3  4C 25 2E 94
0510  04 29 00 00  28 03 5D 90  F1
.E 500
ABCDEFGHIJKLMNOPQRSTUVWXYZ0123456789!"#$%&'():*-=@+;<,?/>
.D 500,518
******************
S0500
X20FF0B5434567 1B6F
X1B2803F34C252E94F
X0429000028035D907
XF1000000000000000
******************
.L

.B 514
.E 500

.T FFB0,*+F
FFB0  A0 2A 05 00  0D 05 14 28  03 5D 90 03  FE 10 41 3F
.T R,P+3F
FFC0  FF FF FF FF  FE C1 FF FF  FF 00 FF FF  05 0C 05 00
FFD0  A4 A0 80 00  A0 A0 A0 20  A0 84 20 80  A0 80 80 02
FFE0  FF FF FF FF  FF FF FF FF  FF FF FF FF  FF FF FF FF
FFF0  80 20 80 80  00 A0 A0 80  20 24 A0 A0  20 20 20 41
.E 500
EXECUTE RESTORED USER CODE REPLACED BY BREAKPOINT
.H 2+0+F+F+0+B+5+4+3+4+5+6+7+1+B+6=005F    CHECKSUM COMPUTED.
.P 01
1 00 FF
```

HEX CODE	CHAR	HEX CODE	CHAR	HEX CODE	CHAR	HEX CODE	CHAR
00	NUL	20	SP	40	@	60	`
01	SOH	21	!	41	A	61	a
02	STX	22	"	42	B	62	b
03	ETX	23	#	43	C	63	c
04	EOT	24	$	44	D	64	d
05	ENQ	25	%	45	E	65	e
06	ACK	26	&	46	F	66	f
07	BEL	27	'	47	G	67	g
08	BS	28	(	48	H	68	h
09	HT	29	)	49	I	69	i
0A	LF	2A	*	4A	J	6A	j
0B	VT	2B	+	4B	K	6B	k
0C	FF	2C	,	4C	L	6C	l
0D	CR	2D	–	4D	M	6D	m
0E	SO	2E	.	4E	N	6E	n
0F	SI	2F	/	4F	0	6F	o
10	DLE	30	0	50	P	70	p
11	DC1	31	1	51	Q	71	q
12	DC2	32	2	52	R	72	r
13	DC3	33	3	53	S	73	s
14	DC4	34	4	54	T	74	t
15	NAK	35	5	55	U	75	u
16	SYN	36	6	56	V	76	v
17	ETB	37	7	57	W	77	w
18	CAN	38	8	58	X	78	x
19	EM	39	9	59	Y	79	y
1A	SUB	3A	:	5A	Z	7A	z
1B	ESC	3B	;	5B	[	7B	{
1C	FS	3C	<	5C	\	7C	I
1D	GS	3D	=	5D	]	7D	}
1E	RS	3E	>	5E	^	7E	~
1F	VS	3F	?	5F	←	7F	DEL

GEMS-8 MICROCOMPUTER SYSTEM

MOSTEK

GEMS-8 MICROCOMPUTER SYSTEM WITH 12K x 8 RANDOM ACCESS MEMORY



Mostek Complete Microcomputer Support Package

GENERAL

The GEMS-8 (General Evaluation Microcomputer System) is an advanced 8-bit microcomputer with a complete package of support software and documentation (Ref. Fig. 1). This system has been carefully designed for OEM applications which might otherwise require the use of a mini-computer or large amounts of random logic. It is also a very attractive alternative for the potential microprocessor user who wishes to avoid the long delays and expenses associated with developing a custom microcomputer system.

MK 5065 MICROPROCESSOR

The heart of the GEMS-8 is the MOSTEK MK 5065 microprocessor. chip. The MK 5065 is a high speed 8-bit microprocessor with an advanced architecture and 51 basic instructions (81 instructions including modifications). Its other features include a unique triple level architecture for extremely fast interrupt response, direct addressing of 32K x 8 of memory, and the ability to address 16 separate peripheral devices.

GEMS-8 PROCESSOR BOARD

The MK 5065 CPU is located on the GEMS-8 processor board. This board contains the additional circuitry necessary to create a complete, stand alone microcomputer. As seen in the block diagram in Figure 2, this board includes 1K x 8 of RAM storage, sockets for 1K x 8 each of PROM and ROM storage, and a complete TTY interface with a punched tape reader step feature. Also included on the board is the additional interface circuitry necessary for adding more memory and peripherals to the system.

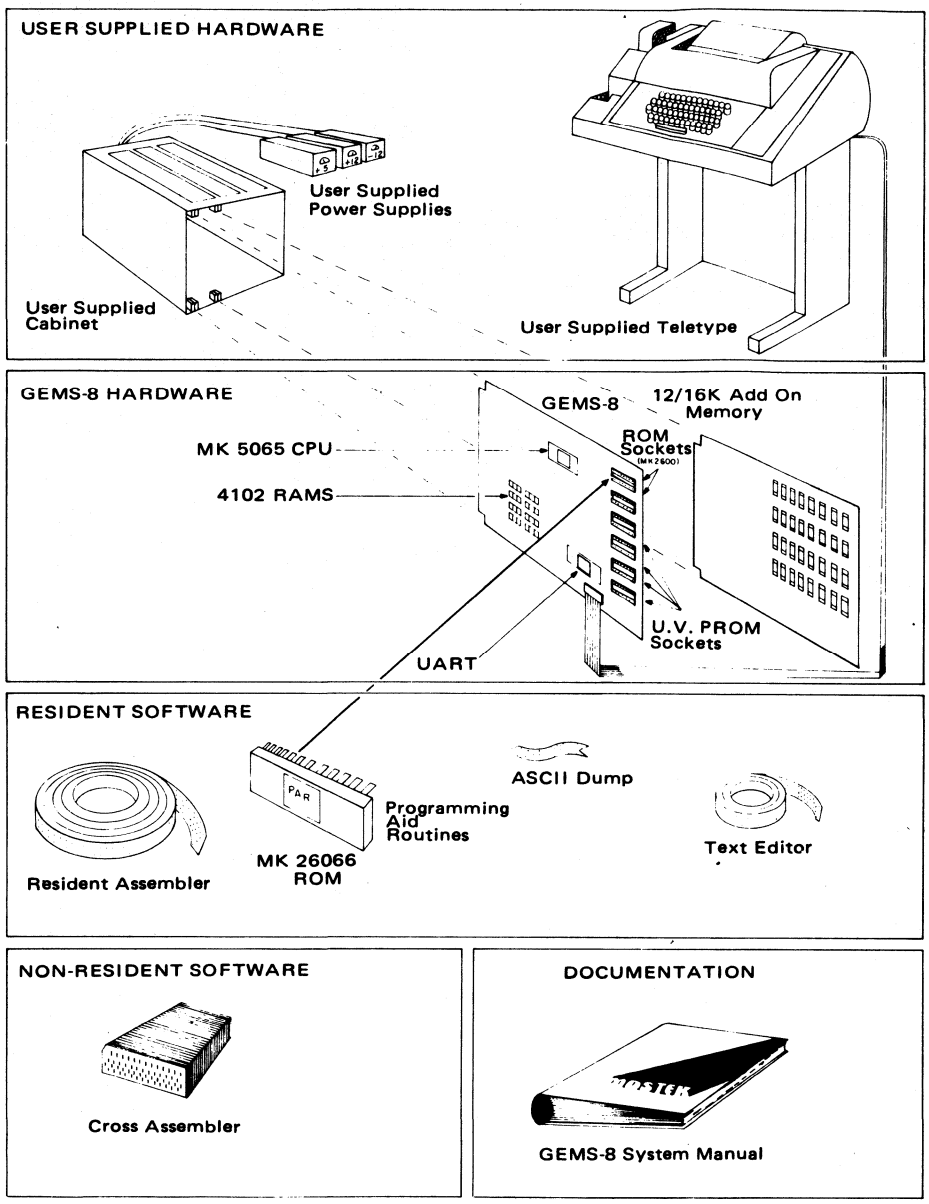


Figure 1. Gems - 8 Development System.

The basic intelligence for the GEMS-8 processor board is contained in the Programmers Aid Routines (PAR) which resides in a 512 x 8 bit ROM memory. This ROM chip is included with the processor board, and plugs into one of the two ROM sockets provided. PAR contains all the software necessary to perform the following functions:

- Examine and/or modify the contents of memory
- Load either binary or ASCII tapes from the TTY
- Transfer control to a previously loaded program for execution
- Set "Break Points" or "Traps" to aid in program debugging

Once the user has developed the particular software for his application, he can place it into either U.V. erasable PROM or a MK 2600 mask ROM. With either of these options, the user will have up to 1K x 8 bits of non-volatile program storage available on the GEMS-8 processor board.

This 1K x 8 bits of ROM/PROM storage, together with the 1K x 8 bits of on board RAM storage, can perform many complex functions which might otherwise have required the user of a complete mini-computer.

GEMS-8 12K/16K MEMORY BOARD

For applications requiring more RAM storage than the 1K x 8 bits included on the processor board, an add-on memory board has been developed. The board can be ordered in either a 12K x 8 or 16K x 8 configuration. Two of the 12K x 8 boards can be used in a single system to provide a total of 24K x 8 bits of RAM storage.

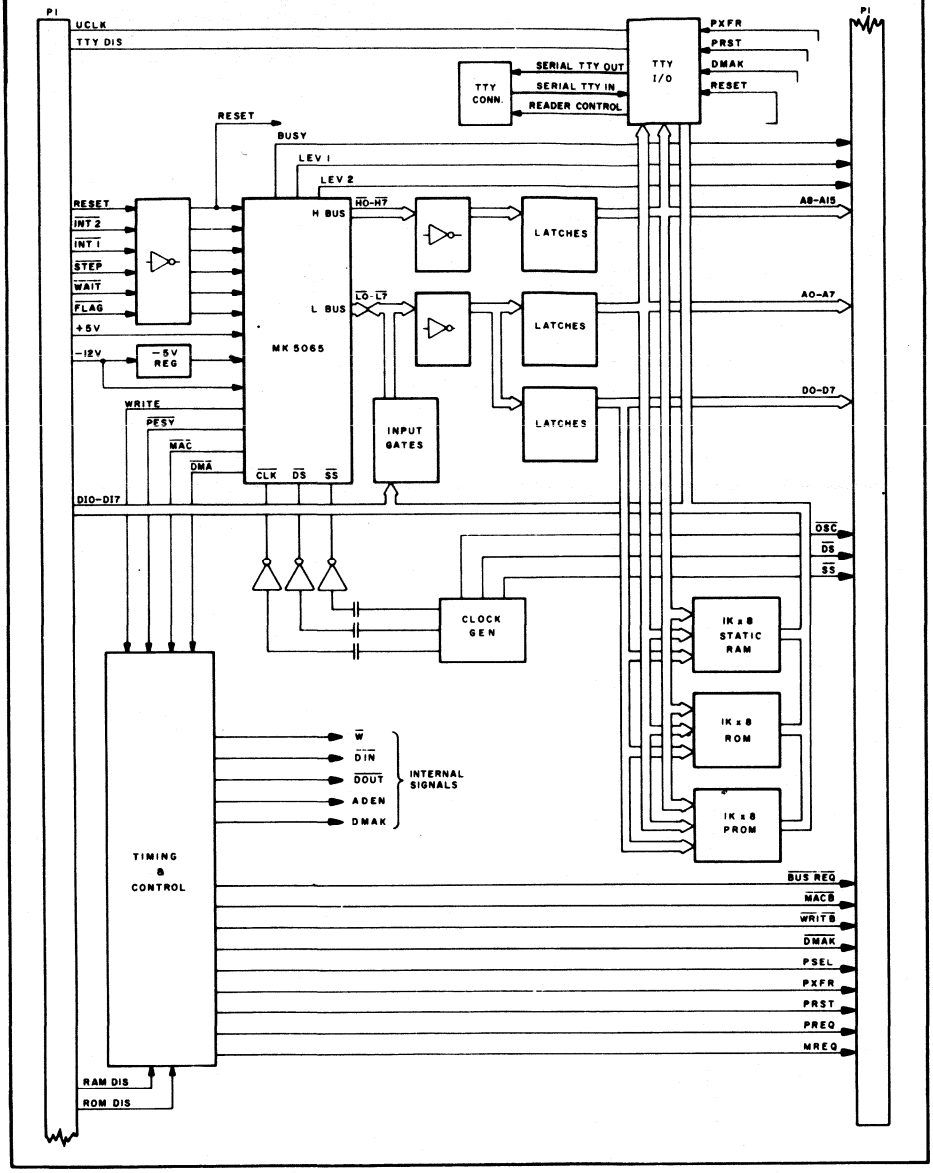
In addition to the advantage of being able to execute longer programs, the availability of a larger memory can greatly simplify program development. This is because a larger memory permits the user of a resident assembler and resident text editor to eliminate the tedious and time consuming tasks of manually assembling and editing source tapes.

RESIDENT SOFTWARE

The resident software which has been written for the GEMS-8 is intended to provide all of the development aids which will be required by the user for developing his particular applications program. This software includes a text editor, assembler and PAR.

The text editor provides a very flexible means for generating and editing the assembly language "source" tape for a program. The assembler is then used to convert this source tape into a corresponding binary or "object" tape which can be loaded directly into the GEMS-8 memory for execution. PAR can then be used to execute and debug the program. When an error is located the object program can either be "patched" in memory using PAR, or the original source tape can be corrected, reassembled, and the new object tape reloaded.

FUNCTIONAL DIAGRAM
GEMS-8 PROCESSOR BOARD



Listings are also available for other miscellaneous routines and sample programs, including an ASCII dump routine for storing a designated protion of memory onto a paper tape in ASCII format.

NON-RESIDENT SOFTWARE

For the user who has access to a computer system capable of supporting Fortran IV, a non-resident assembler is available. This program is supplied as a card deck containing the Fortran IV source for the non-resident assembler.

DOCUMENTATION

One of the most essential development aids required by a microcomputer user is the system documentation. Because of this, a great deal of effort has gone into the planning and generation of the GEMS-8 system manual. Included in the manual are the following:

- System operating guide — a self contained description of basic system operating techniques, including a detailed step by step example of manually assembling, loading and executing a sample program
- Programming guides — contains a detailed explanation of all "true" and pseudo instructions in the MK 5065 assembly language as well as a description of the many advanced programming techniques possible.
- GEMS-8 hardware section — describes in detail each of the system hardware elements including schematics and circuit descriptions.
- GEMS-8 software section — describes in detail each of the system software elements, including operating instructions and source listings.

SPECIFICATIONS

Operating Temperature Range -
O ° C To 50 ° C

Power Supply Requirements -
MicroProcessor Board -
+5V @ 2.5A
−12V @ 1.0A

12K/16K Memory Board
+5V @ 1.5A
+12 @ 0.5A
−12 @ 50mA

System Clock Rate
4.0MHz

Board Size
9.6" x 6.75"

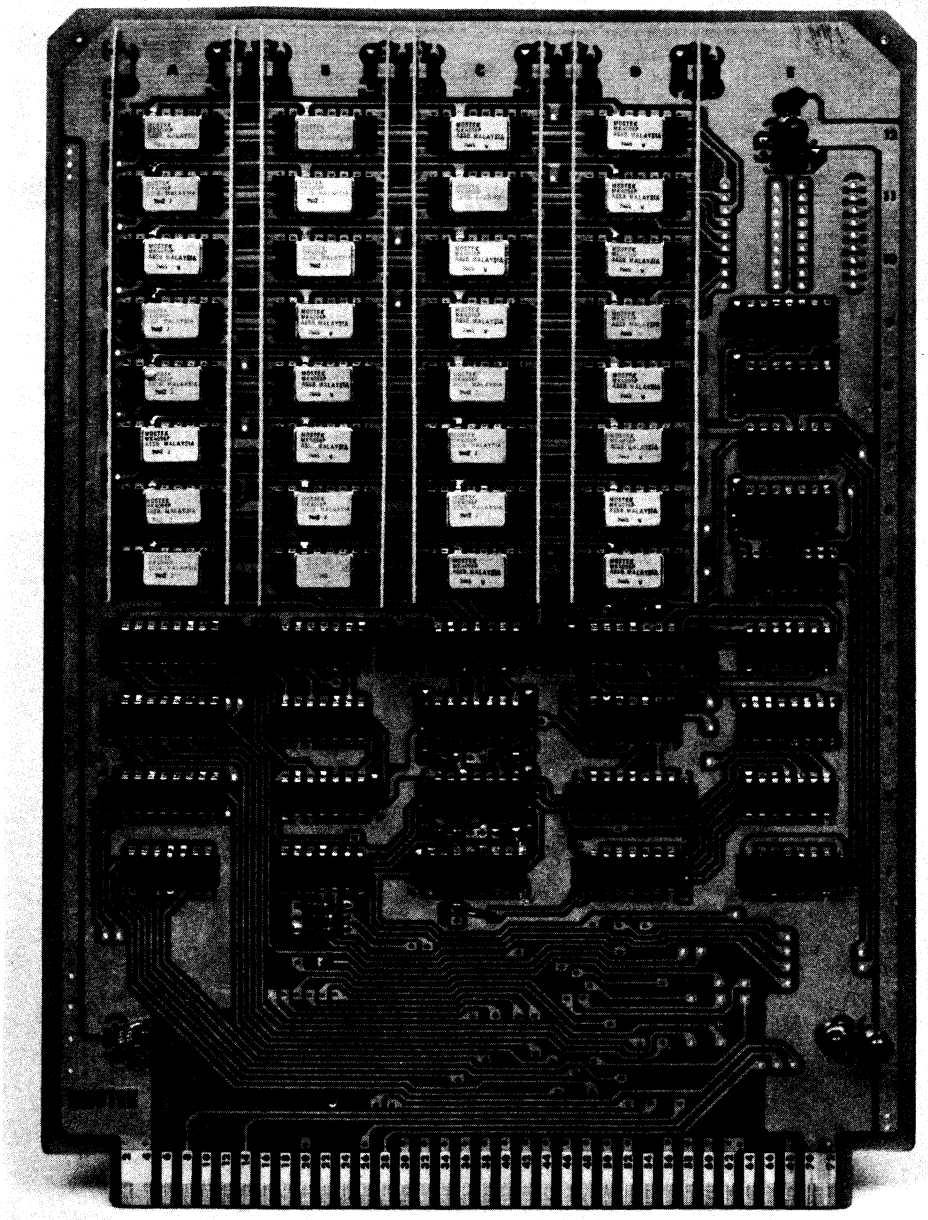
72 Ping Card Edge -
Connector Pins On -
.156 inch Centers

12/16K Memory System

MOSTEK

MICROPROCESSORS

12/16K Memory System for the MK5065 Microprocessor



INTRODUCTION

The key to saving engineering man hours and unnecessary hardware in the design of microprocessor oriented products is to have a good development system and all of the necessary software to make the design task easier. The intent of this paper is to describe an add-on memory system which interfaces with the MOSTEK MK 5065 microprocessor chip. The system is available in printed circuit board form and is designated the MOSTEK 5065-4096-3K MEMORY SYSTEM. The board can utilize either MK 4096 4K or the lower cost MK 4096-31 (32/33/34) 3K dynamic RAM chips. When fully populated with 32 RAM chips, the board provides a memory capacity of either 16K x 8 bits (with 4K RAMs) or 12K x 8 bits (with 3K RAMs). To avoid confusion, only the 12K version of the board will be discussed here.

DESIGN REQUIREMENTS

The main requirement of this memory system is to provide high performance READ/WRITE storage for any MK 5065 microprocessor system. To accomplish this goal the MEMORY ADD-ON BOARD is designed such that it contains the following strappable options and features:

1. Direct Interface with MK 5065* This memory system requires only 4 control signals from the CPU.
   A. $\overline{OSC}$ – Free-running oscillator used to generate all system clocks. OSC frequency ⩽ 4 MHz.
   B. $\overline{State\ Strobe}$ – One of the three system clocks.
   C. $\overline{MAC}$ – 5065-generated signal, signifies a memory cycle.
   D. $\overline{WRITE}$ – 5065-generated signal, signifies a memory write cycle.

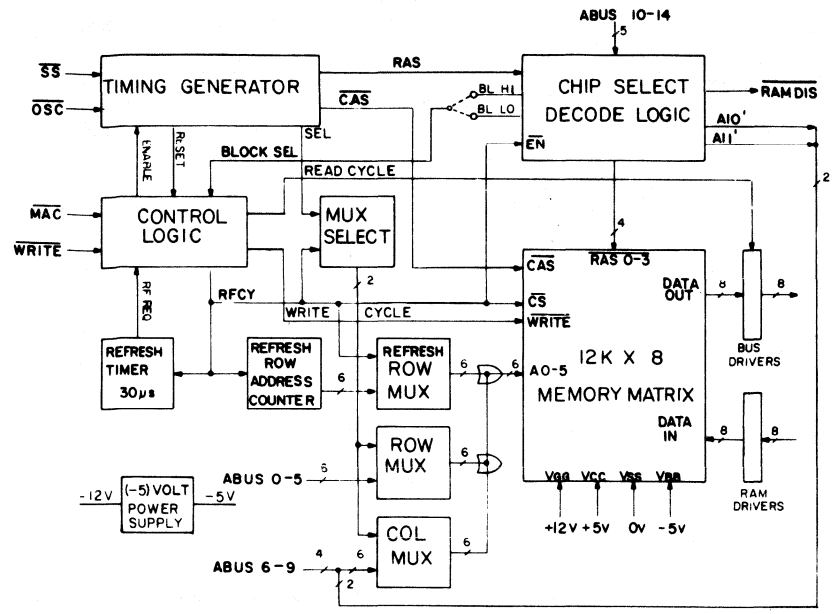
2. DMA Capability – With the processor in the "WAIT" mode, direct access of the memory can be accomplished by providing control signals similar to those generated by the MK 5065. The maximum DMA rate should not exceed .5 MHz.

3. "Cycle Steal" Refresh – Because of the dynamic nature of the memory parts, the memory system must initiate one refresh cycle every 32 microseconds. The time between refresh cycles is controlled by the refresh timer one-shot. When the one-shot times out, the memory controller will "steal" one-half of the next available cycle. This type of refresh is very efficient.

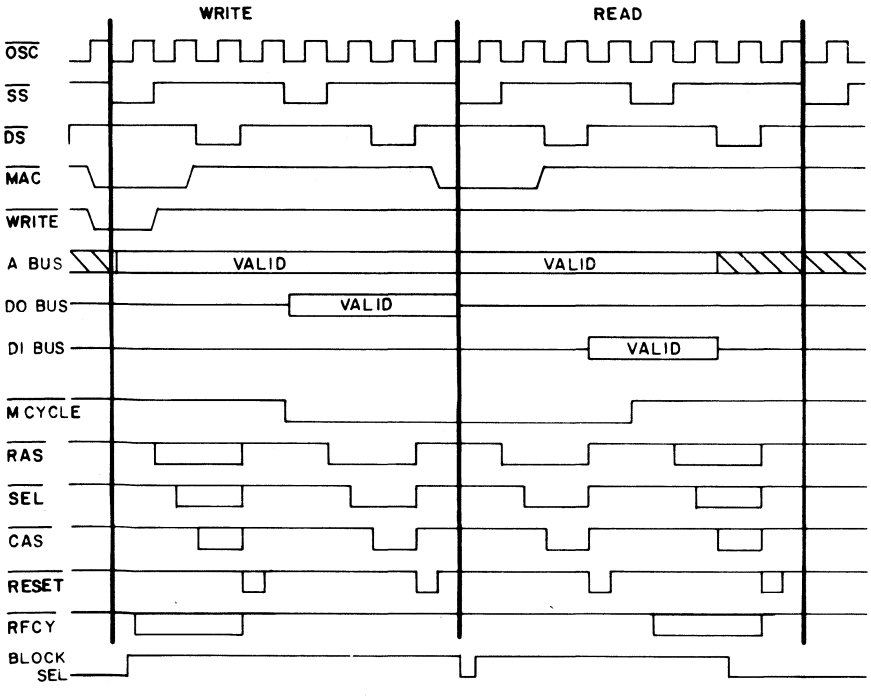
4. Low Power Mode of Operation – The power required by the RAMs in the memory matrix is substantially reduced by applying power only to selected chips. This is accomplished by decoding the ROW ADDRESS STROBE signal and using it as a chip select for the RAMs. This mode of operation reduces power required by the RAMs from approximately 4 watts to approximately 1.1 watts average. Total memory system power is less than 4.5 watts typical.

5. On Board (–5V) Power Supply – Required by the RAMs and is generated from the –12V supply used for the CPU Board.

6. Bi-Directional Data Bus Option – The DATA BUS out of the matrix is a three-state bus. It is enabled only during a READ CYCLE. Therefore, in applications requiring a bi-directional bus, the DATA-IN and DATA-OUT BUSSES may be wired together as long as no other device drives the bus during a READ CYCLE.

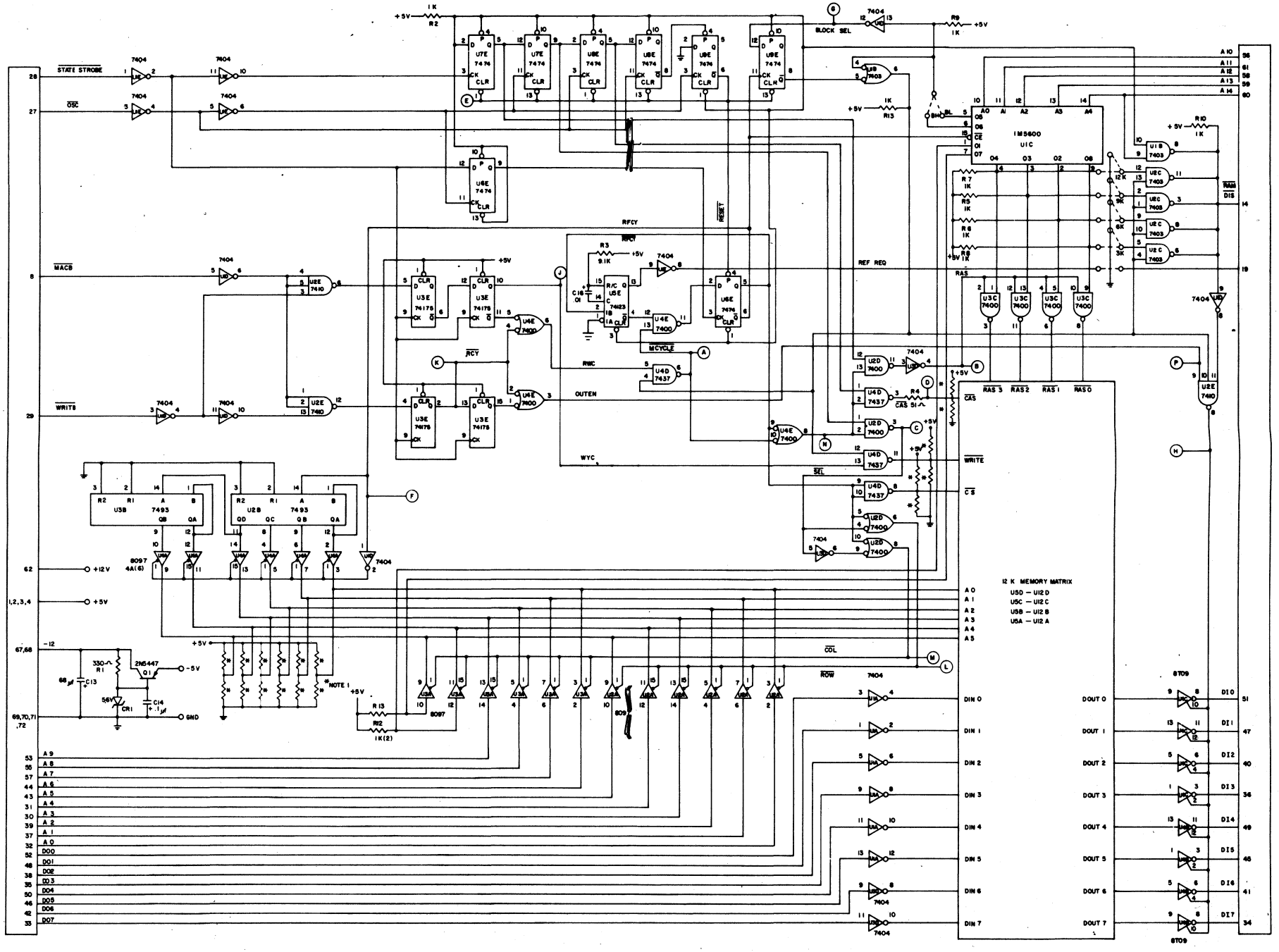


FUNCTIONAL DIAGRAM



INTERFACE TIMING

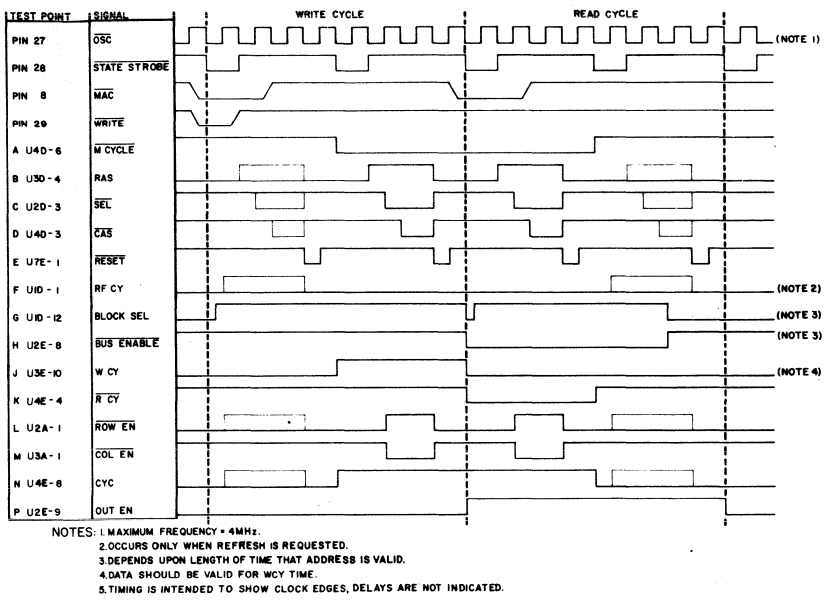
*This assumes addresses and data vlaid for sufficient time for the memory system by means of latches in the CPU.


STATE STROBE
OSC
MACB
WRITE
WRITE
RFCY
REF REQ
RAS
RAS DIS
BLOCK SEL
RESET
MCYCLE
RWC
OUTEN
WYC
SEL
CAS
CAS
WRITE
CS
RAS 3
RAS 2
RAS 1
RAS 0
ROW
COL
IM5600 U1C
12 K MEMORY MATRIX
U5D — U12D
U5C — U12C
U5B — U12B
U5A — U12A
NOTE 1
+12V
+5V
-12
-5V
GND
DIN 0
DIN 1
DIN 2
DIN 3
DIN 4
DIN 5
DIN 6
DIN 7
DOUT 0
DOUT 1
DOUT 2
DOUT 3
DOUT 4
DOUT 5
DOUT 6
DOUT 7
A 0
A 1
A 2
A 3
A 4
A 5
A 9
A 8
A 7
A 6
A 5
A 4
A 3
A 2
A 1
A 0
D00
D01
D02
D03
D04
D05
D06
D07
A 10
A 11
A 12
A 13
A 14
DI0
DI1
DI2
DI3
DI4
DI5
DI6
DI7

7. Strappable Options — This board can be populated from 3K to 12K bytes in 3K increments. RAS0-RAS3 serve as Chip Select signals for the RAMs. By removing the desired "jumpers" on the board, the RAM DISABLE signal can be programmed to activate only when the populated portion of the memory matrix is addressed.

   A. Low, Hi Board Select — Allows the memory to occupy either 0-12K or 13K-24K locations.

   B. RAM DISABLE — This is an open-collector output which disables any other RAM when the 12K board is selected.



INTERNAL SYSTEM TIMING

CIRCUIT OPERATION

In this memory system the memory storage is implemented with MK 4096-31/32/33/34 Random Access Memory circuits. These are functionally equivalent to the MK 4096 except that one quadrant* in the memory can not be legally addressed thus making it a 3072 (3K) bit memory.

The following chart defines the illegal quadrant* in the 4096-31/32/33/34 RAM.

Part No.	Column Address A5	Column Address A4
4096-31(A)	1	1
4096-32(B)	1	0
4096-33(C)	0	1
4096-34(D)	0	0

The function of the memory controller is to interface the MK 4096 memory parts to the MK 5065 microprocessor. The controller must accept control signals directly from the processor and initiate either READ or WRITE cycles upon request. The controller must also initiate REFRESH cycles for the memory in such a way that they are "hidden" from the processor.

*(The illegal quadrant is determined by the 2 highest order column address bits.)

The memory controller itself is totally synchronous. All timing signals are generated by a shift register which is clocked by the main oscillator (OSC) in the CPU. (A typical circuit for generating system clocks is shown in Figure A.) To change the rate of operation of the entire system, one changes the frequency of the main oscillator. All signals will maintain their relationship to each other.

MEMORY CYCLES

A memory cycle occurs when the processor outputs a MAC signal to the memory. At the same time the processor will also indicate whether the cycle will be a READ or WRITE operation. The memory controller uses the leading edge of STATE STROBE (see timing) to latch this information and start a memory cycle. Before any of the control signals are generated and applied to the memories, certain conditions such as address decode and multiplexing must be set up.

DECODING

Decoding address bits for a 12K memory system may seem difficult at first glance. In this system, a 32 x 8 PROM is employed to take the complexity out of this task. It also permits many features to be

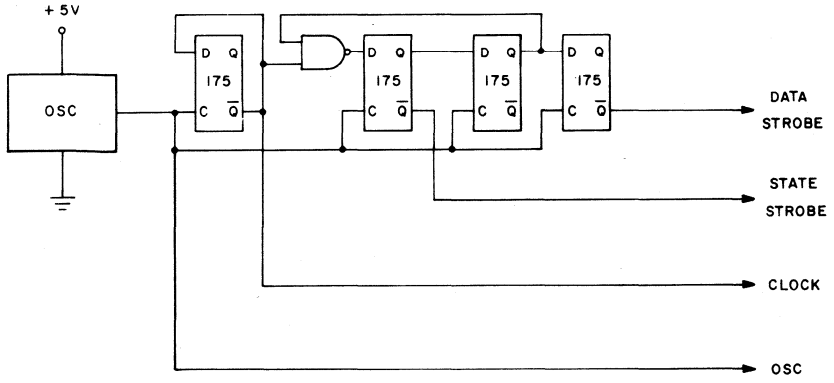


Figure A

implemented that would be very difficult to design into a standard decoder. This decoding scheme assumes that every 3K x 8 bit block of memory is implemented with the same type of 3K RAM. All RAMs in that block must have the same illegal quadrant.

The five highest order address bits are used to address the ROM DECODER. Four outputs of the ROM are used as 3K BLOCK ENABLES for the memory matrix. Two more outputs are used to indicate which 12K block of memory is enabled in the overall memory map.

1. BLOCK LOW: activated when any location from 0-12K is addressed.

2. BLOCK HI: activated when any location from 13K-24K is addressed.

The four block enable outputs from the ROM are "ANDed" with the ROW ADDRESS STROBE to enable only one selected 3K block of memory. Since only one block of dynamic memory (eight 3K RAMs) has active power applied to it at a time, the overall system power is substantially reduced.

With this type of decoding, construction of continuous memory array becomes very easy. Also, it allows the board to be partially populated in 3K byte increments.

MULTIPLEXING

Because of the unique design of MOSTEK's 4K RAM, it can be packaged in a 16 pin DIP. This results in much greater packing density than any other 4K RAM. Twelve address bits are required to select one of the 4096 bits (in this case 3072 bits) in each memory circuit. Since there are only six address inputs to the MOSTEK RAM, the addresses must be multiplexed into the chip.

Three sets (6 each) of TRI-STATE bus drivers are used for multiplexing the ROW, COLUMN and REFRESH ROW ADDRESSES onto the six memory address inputs in the matrix. During a normal memory cycle the ROW ADDRESSES are enabled first.

After allowing ample time for these addresses to reach proper logic levels, the ROW ADDRESS STROBE occurs and latches these address bits into the RAMs. After a minimum hold time of 80 nanoseconds, the SELECT signal occurs, disabling the ROW ADDRESS and enabling the COLUMN ADDRESS onto the matrix. The COLUMN ADDRESS STROBE is generated to latch these addresses into the RAMs.

During a REFRESH CYCLE both ROW and COLUMN ADDRESSES are disabled and only the REFRESH ROW ADDRESS COUNTER is enabled.

REFRESH CYCLES

Because the memory elements in this system are high performance, dynamic circuits, refreshing is required every 2 milliseconds or less. This is accomplished by performing one READ cycle every 30 microseconds with all memory circuits unselected. To make this action transparent to the CPU, refreshing is done on a "Cycle Stealing" basis.

In the memory controller, a retriggerable one-shot is adjusted to have a pulse width of 30 microseconds. When this refresh timer times out, a REFRESH REQUEST signal is supplied to the memory control logic. At the next possible time slot that the CPU is not exercising the memory, a REFRESH CYCLE is executed.

During a REFRESH CYCLE, Chip Select (CS) is disabled, unselecting the RAMs. Also Chip Enable (CE) to the DECODER ROM is removed, causing all of the open-collector outputs to be pulled high. The REFRESH ROW ADDRESS COUNTER drivers are enabled, allowing the REFRESH ROW ADDRESS to be supplied to the memory matrix. RAS and CAS are generated as if this was a normal read cycle. At the end of a REFRESH CYCLE the REFRESH ROW ADDRESS COUNTER is incremented and the REFRESH TIMER is retriggered.

The REFRESH CYCLE can be summarized as the application of the ROW and COLUMN ADDRESS STROBES to all RAMs in the matrix with none of the RAMs enabled.

RAM DISABLE OUTPUT

This is an open-collector, active low, output that can be used to disable any other device connected to the DATA BUS when this 12K memory board is addressed by the processor. If a partially populated memory matrix is desired, on-board jumper straps can be removed to prevent this output from becoming active at the wrong time.

GENERAL

The design of this 12K ADD-ON MEMORY for the MK 5065 assumes that the CPU section of any processor or mini-computer utilizing the MK 5065 microprocessor contains address and data latches to hold this information valid for a sufficient time required by the MK 4096 RAMs.

Recommended Power Supplies for the System:

V_{CC} = +5 volts @ 1.5 amps
V_{GG} = +12 volts @ .5 amps
V_{BB} = −5 volts @ 10 mA

Also available from MOSTEK is a GENERAL EVALUATION MICROCOMPUTER SYSTEM (GEMS-8) P. C. Board utilizing the MK 5065 Microprocessor. For further information and current pricing on any MOSTEK product please write:

MOSTEK GmbH

7024 Filderstadt 1
Talstraße 172

If you would like to be included on our mailing list for additional micor-processor support information, please fill out the form and return to:

MOSTEK GmbH
7024 FILDERSTADT, TALSTRASSE 172
Telefon: (07 11) 70 10 96, Telex: 7 255 792 MKD

NAME _____

COMPANY NAME _____

COMPANY ADDRESS _____

CITY _____

STATE _____ ZIP CODE _____

MAIL STATION _____

PHONE _____

Type of Application (Leave Blank If Unknown)

☐ Test equipment on instrumentation

☐ Data terminals, P.O.S., communications, peripheral controller

☐ Office and business machines (including calculators)

☐ Military systems

☐ Industrial control

☐ Education or consumer

☐ Medical

☐ Other _____

MEMORIES
MICRO-
PROCESSORS
CONSUMER
CIRCUITS
INDUSTRIAL
FUTURE
PRODUCTS

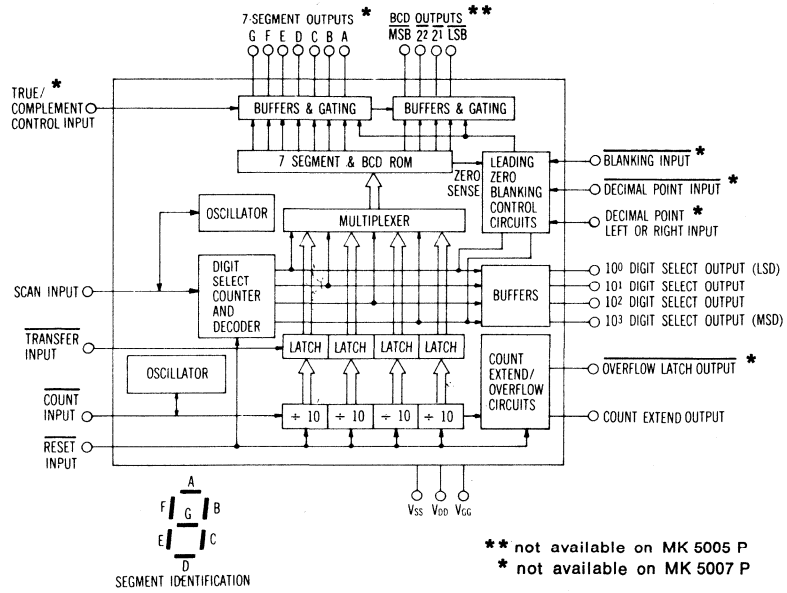
MOSTEK

MOS 4-Digit Counter/Display Decoder

MOSTEK

INDUSTRIAL

FUNCTIONAL DIAGRAM



** not available on MK 5005 P
* not available on MK 5007 P

GENERAL DESCRIPTION

The MK 5002/5/7 P is an ion-implanted, P-channel MOS four-decade synchronous counter with latches, multiplexing circuits, and a read-only memory programmed for seven-segment outputs and BCD outputs. In addition, many on-chip control circuits provide flexibility of use with a minimum of external components.

The MK 5002/5/7 P provides a means of counting up to 9999, transferring the count into latches without interrupting the counting operation, and supplying the latched information to the outputs one decade at a time. Scanning is controlled by the Scan Input which increments a one-of-four counter on its negative edge, thereby scanning the latches from MSD (Most Significant Digit) to LSD (Least Significant Digit).

Low threshold voltages for input DTL/TTL compatibility are achieved through Mostek's ion-implantation process. Enhancement mode, as well as depletion-mode, devices are fabricated on the chip, allowing it to operate from a single +5V power supply. Depletion-mode technology also allows the entire circuit to operate on less than 25 mW of power.

The functional diagram shows all options available on the MK 5002 P MOS/LSI. Other members of this family which are different pin-outs of this same chip are the MK 5005 P and MK 5007 P. The MK 5005 P is supplied in a 24 pin package and does not include the BCD outputs. The MK 5007 P is supplied in a 16 pin package. (See the pin diagrams for these members of the counter/display decoder family.)

TRUTH TABLES

INPUT TRUTH TABLE

Input	Logic Condition to Activate
$\overline{\text{Count}}$	Negative Edge
$\overline{\text{Reset}}$	0
$\overline{\text{Transfer}}$	0
Scan	1 (Negative Edge increments Digit Select Counter)
True/Complement	1 = True Data 0 = Complementary Data
$\overline{\text{Decimal Point}}$	0
$\overline{\text{Blanking}}$	0
Decimal Point Left or Right	1 = Left 0 = Right

7-SEGMENT & BCD OUTPUTS TRUTH TABLE

Digit	Scan	DISPLAY SEGMENT a	b	c	d	e	f	g	BCD $\overline{\text{MSB}}$	$\overline{2^2}$	$\overline{2^1}$	$\overline{\text{LSB}}$
0	1	0	0	0	0	0	0	1	1	1	1	1
1	1	1	0	0	1	1	1	1	1	1	1	0
2	1	0	0	1	0	0	1	0	1	1	0	1
3	1	0	0	0	0	1	1	0	1	1	0	0
4	1	1	0	0	1	1	0	0	1	0	1	1
5	1	0	1	0	0	1	0	0	1	0	1	0
6	1	0	1	0	0	0	0	0	1	0	0	1
7	1	0	0	0	1	1	1	1	1	0	0	0
8	1	0	0	0	0	0	0	0	0	1	1	1
9	1	0	0	0	0	1	0	0	0	1	1	0
X	0	1	1	1	1	1	1	1	1	1	1	1

True/Complement = Logic 1

TRUTH TABLE, OTHER OUTPUTS

Output	True Logic State	Time of Occurrence
Digit Select Outputs	1	One-of-four, following Scan Input rising edge; all off when Scan Input is low.
$\overline{\text{Overflow Latch}}$	0	Occurs on the 10,000th Count Input following a reset. Remains true until an external reset is accomplished.
Count Extend	1	Occurs each time the counter state attains 9,999 count. Remains true only until the next Count Input or Reset occurs (when the counter returns to 0,000).

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
T_A	Operating Temperature Range	0		75	°C	
V_{SS}	Supply Voltage	4.5		7.5	V	1, 2
V_{GG}	Supply Voltage	V_{DD}		-13.2	V	1, 2

ELECTRICAL CHARACTERISTICS

($V_{SS} = +5V \pm 5\%$; $V_{GG} = V_{DD} = 0$ V; $0° C \leq T_A \leq 70° C$ unless otherwise noted)

		PARAMETER	MIN	TYP	MAX	UNITS	NOTES
D. C. CHARACTERISTICS	V_{IL}	Input Voltage, Logic 0 (Low)		V_{DD}	$V_{DD}+0.8$	V	
	V_{IH}	Input Voltage, Logic 1 (High)	$V_{SS}-1$	V_{SS}	$V_{SS}+0.3$	V	3
	I_{SS}	Supply Current, V_{SS}		2.5	5.0	mA	4, Inputs open
	I_{GG}	Supply Current, V_{GG}		0.2	0.5	mA	V_{GG}=-12V
	C_{in}	Input Capacitance		3	10	pF	T_A=25°C; f=1MHz; $V_{IN}=V_{SS}$
	I_{IL}	Input Current, Logic 0, Count Input			1.6	mA	5
		Scan Input			1.6	mA	5
		Decimal Point Input			1.0	µA	
		Other Logic Inputs			1.0	mA	
	I_{OL}	Output Current, Logic 0	0.5			mA	6, V_{GG}=-12V
	I_{OH}	Output Current, Logic 1	0.5			mA	6, V_{GG}=-12V
	V_{OL}	Output Voltage, Logic 0			$V_{DD}+0.2$	V	4
	V_{OH}	Output Voltage, Logic 1	$V_{SS}-0.2$			V	4
DYNAMIC CHARACTERISTICS	f_{CI}	Count Input Frequency	DC		250	KHz	
	f_{SI}	Scan Input Frequency	DC		50	KHz	
	t_{RD}	Reset to Any Output Delay			15	µs	
	t_{PW}	Logic 0 Pulse Width, Reset Input	1.0			µs	
		Count Input	1.0			µs	
		Scan Input	10.0			µs	
		Transfer Input	2.5			µs	
	t_{PH}	Logic 1 Time, Count Input	3.0			µs	
		Scan Input	10.0			µs	
	t_{SD}	Scan to Output Disable Time, Digit Select Outputs			15	µs	7
		All Data Outputs			15	µs	7
	t_{SE}	Scan to Output Enable Time, Digit Select Outputs			15	µs	8
		All Data Outputs			15	µs	8
	t_{CE}	Count Input to Count Extend Delay to 1 or 0			15	µs	9
	t_{OF}	Count Input to Overflow Delay (On)			15	µs	9
	t_{ROF}	Reset Input to Overflow Delay (Off)			5	µs	

NOTES:
1. V_{DD} = 0 V
2. V_{SS}/V_{GG} differential no more than 25 V.
3. Internal pull-up resistors (approx 10 K Ohm) are provided at all inputs other than Count Input, Scan Input, & Decimal Point Input.
4. V_{GG} = -12V ± 10%. Outputs open.
5. Measurement made at $V_I = V_{DD} + 0.4$ V. This condition is sufficient to represent a logic 0 and hold off or override the internal oscillators. Maximum current at V_I = +0.4V is 1.6 mA. 400 µA source current at V_{SS}-1.0 is sufficient to represent a logic 1 and hold off or override the internal oscillators.
6. I_{OL} measured at $V_O = V_{SS} - 0.75$ V. I_{OH} measured at $V_O = V_{DD} + 0.75$ V. (See MK 5002 P Application Note for output characteristics.)
7. Delay measured from the negative edge of the Scan Input.
8. Delay measured from the rising edge of the Scan Input.
9. Delay measured from the negative edge of the Count Input.

INDUSTRIAL

DESCRIPTION OF OPERATION

(Further information on the operation of Mostek's family of 4-digit Counter/Decoders may be found in the MK 5002 P Application Report.)

COUNTER LOGIC & TIMING

The Decade counters are *synchronously* incremented on the negative edge of the Count Input. The internal oscillator on this input may be overridden by an external signal source or may be allowed to oscillate at a frequency set by a single capacitor tied to this input from the V_{SS} or V_{DD} supply. In systems with considerable noise, better oscillator stability exists when the capacitor is tied to V_{ss}.

SCAN CONTROL LOGIC & TIMING

The Digit Select Counter is incremented by a negative edge on the Scan Input. During the time the Scan Input is at 0, the 7-segment and Digit Select outputs are forced off and the complement BCD outputs are forced to logic 1. (See Truth Tables.) This remains until the Scan Input returns to logic 1.

The Digit Select Counter is a one-of-four counter, scanning from MSD (Most Significant Digit) to LSD (Least Significant Digit), enabling one quad latch output at a time, and presenting a logic 1 to the corresponding Digit Select output.

The internal oscillator on this input may be overridden by an external signal source or may be allowed to oscillate at a frequency set by a single capacitor tied to this input from the V_{SS} or V_{DD} supply. In systems with considerable noise, better oscillator stability exists when the capacitor is tied to V_{SS}.

TRANSFER LOGIC & TIMING

While the Transfer input is a logic 0, data in the decade counters is transferred to the static storage latches. This input may be left at 0 for a continuous transfer-and-display mode, or may be pulsed periodically to store only on command.

Termination of a transfer command occurs internally when the input is taken to a logic 1 and the next Count Input negative edge occurs. This allows asynchronous Count and Transfer operation since the transfer is terminated prior to incrementing the counters. This means that a Count Input negative edge must follow a Transfer command before a Reset is applied to prevent transfer of invalid data. An external Reset Command must be delayed at least one Count Input negative edge following a Transfer. External transfer should terminate at least 1 μs prior to this Count negative edge and Reset should occur no sooner than 1 μs following that edge.

RESET CONTROL

The decade counters are reset to 0,000 when the Reset Input is at logic 0. The Reset Input at logic 0 also forces the Scan to the MSD output and resets the Overflow Latch output to a logic 1 (if previously latched to a logic 0). It maintains this condition as long as the logic 0 is present at the Reset Input and overrides all other associated inputs. As indicated previously, the decade counters should not be reset until a transfer has been terminated.

Since the Reset Input resets the Scan Counter to MSD the scan rate must be much faster than the reset rate to allow the lesser significant digits to be enabled. Therefore, F_{Scan} must be much greater than four times F_{Reset}.

Ideally, the Reset pulse should also be made narrow, to prevent its duration from causing the MSD to be ON much longer than the other digits and thus appear to be brighter.

LEADING ZERO BLANKING

At the start of each MSD to LSD scan, blanking of leading zeros occurs until the first non-zero number occurs in the display or the Decimal Point Input is clocked. Any number following will be displayed. Leading zero blanking does not affect the BCD outputs or the LSD in the display which is displayed even if zero. The LSD output resets the blanking circuitry to begin blanking zeros in the next scan cycle.

The Decimal Point Input pin should be brought to logic 0 at the time the character is enabled that contains the decimal point. The first non-zero number or the Decimal Point Input signal in the scan cycle puts the blanking circuitry in the unblanking mode. If the Reset In (forces the Scan Counter to the MSD) occurs when the circuit is in the unblanked mode the first complete MSD to LSD scan will be done in the unblanked mode. This could result in a dimly displayed leading zero. A simple solution to this problem would be to force the Blanking Input low during a reset and release it only after an LSD has occurred.

Leading zero blanking may be inhibited by wiring the Decimal Point Input to ground. The MK 5007 P does not have a pin for Decimal Point Input and therefore does not have leading zero blanking.

OTHER INPUTS

The Blanking Input at logic 0 forces the 7-segment outputs to the off-state and the BCD to the equivalent of the number zero. This condition is maintained on a DC basis as long as the Blanking Input is 0. The Digit Select outputs continue to operate at the scan rate as described.

A True/Complement control inverts both BCD and 7-segment outputs when at logic 0. Depending upon the display used, combinations of the Blanking Input and True/Complement Control can be chosen to give a lamp test.

The Decimal Point Left or Right control allows the use of displays with the decimal point physically located on the left or right of the numeral. Logic 1 is decimal-point-right. In the right mode, even though the Decimal point input is clocked, unblanking is delayed until the following digit is enabled.

OUTPUTS

All output buffers on the MK 5002 family are push-pull. A negative power supply terminal, V_{GG}, is provided to increase the drive capabilities of these output buffers. Since the V_{GG} supply is connected only to these output buffers, it has no effect on any other device characteristics.

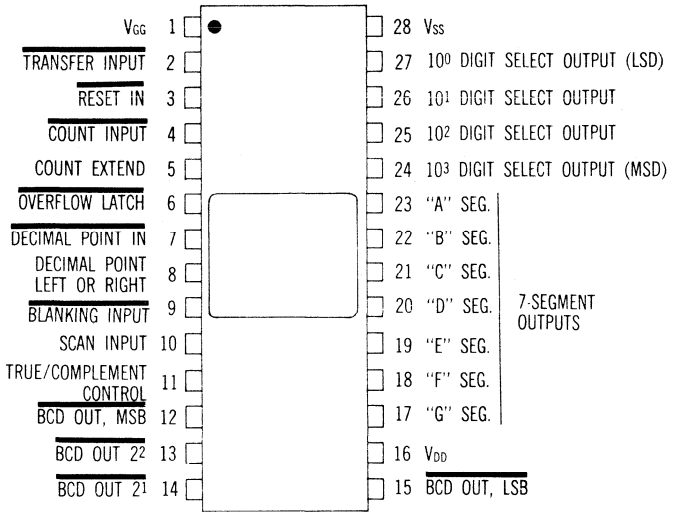
Output characteristics are covered in the MK 5002 Application Report which illustrates the effects of V_{GG} with current to be expected at various output voltages.

The outputs are designed to drive directly to the base of common-emitter transistors, so that output voltage is clamped or maintained at a potential where the MK 5002 P is able to sink or source its greater amount of current.

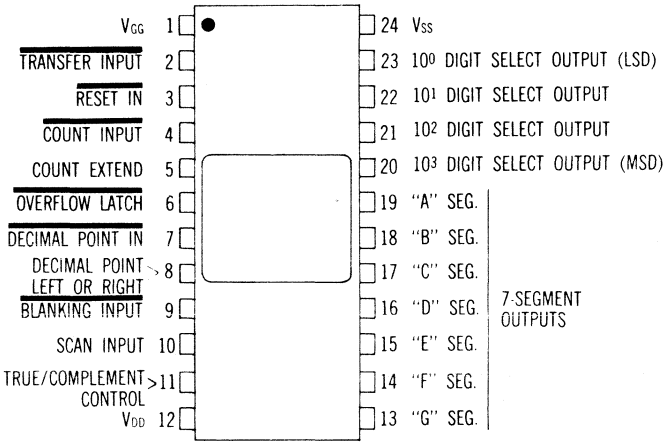
PIN CONNECTIONS

The MK 5002/5/7P is available in a 28-pin dual-in-line package, a 24-pin dual-in-line package, and a 16-pin dual-in-line package. Only the 28-pin package contains all available functions.

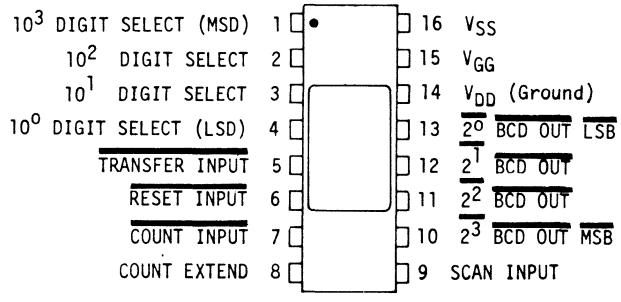
MK 5002P
MK 5002N



MK 5005P
MK 5005N

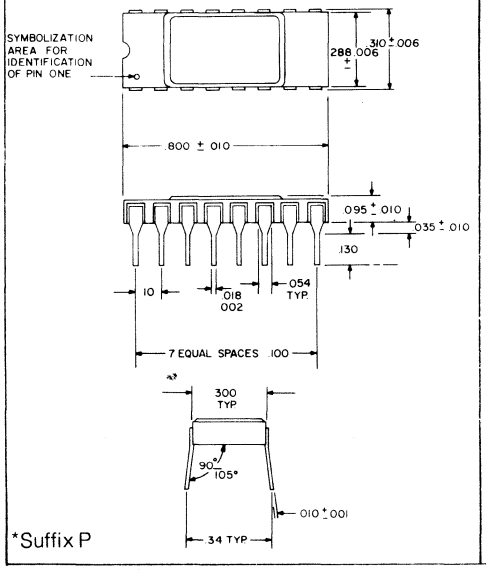


MK 5007P
MK 5007N



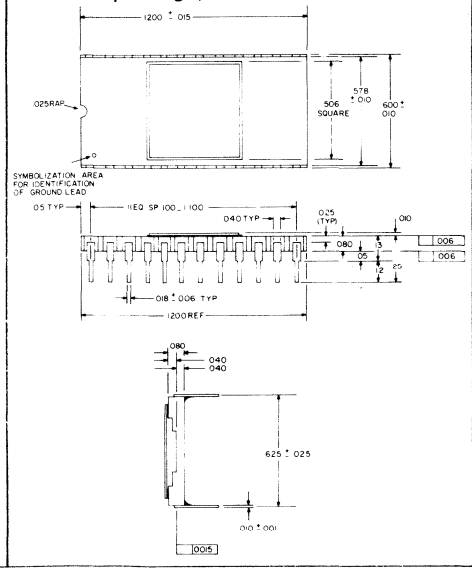
PHYSICAL DESCRIPTIONS

(16-lead ceramic dual-in-line hermetic package)*

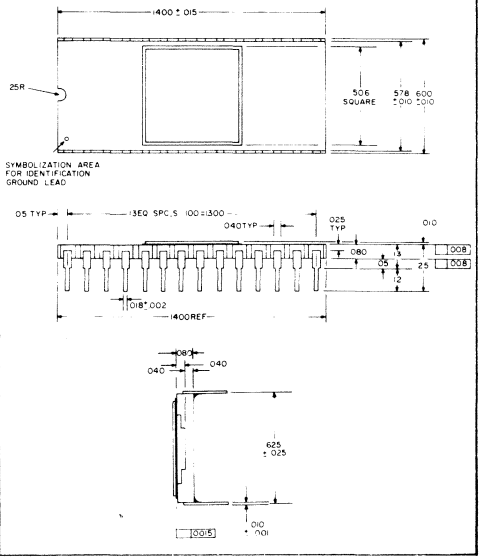


*Suffix P

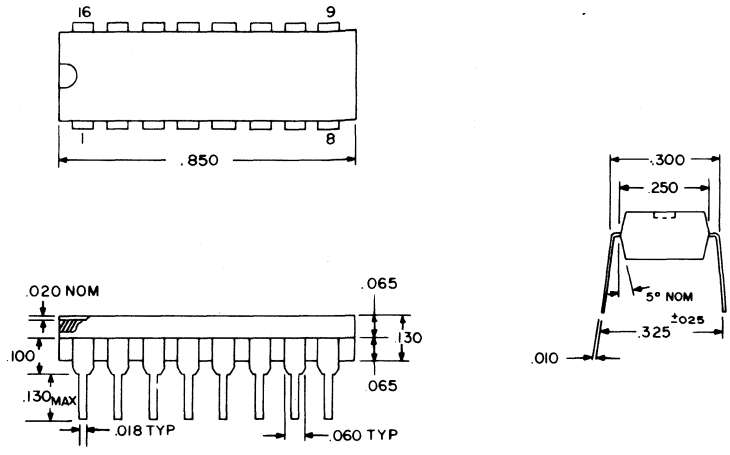
(24 lead ceramic dual-in-line hermetic package)*



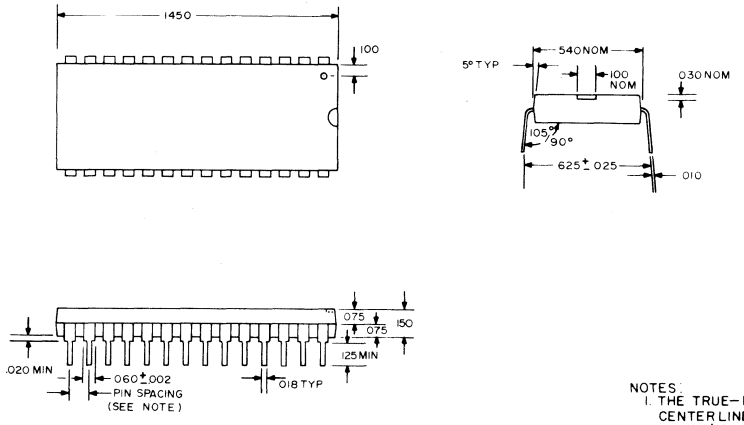
(28 lead ceramic dual-in-line hermetic package)*



PACKAGE 16-pin plastic dual-in-line *



PACKAGE 28-pin plastic dual-in-line *



NOTES:
1. THE TRUE-POSITION PIN SPACING IS 0.100 BETWEEN CENTERLINES EACH PIN CENTERLINE IS LOCATED WITIN ±0.100 OF ITS TRUE LONGITUDINAL POSITION RELATIVE TO PINS 1 AND 28.

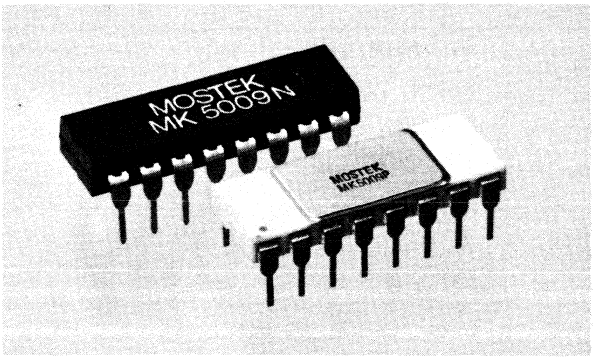
*Suffix N

MK 5009 P
MK 5009 N

MOS Counter Time-Base Circuit

MOSTEK

- ☐ Ion-implanted for full TTL/DTL compatibility
- ☐ Internal clock operates from:
  - External signal
  - External RC network
  - External crystal
- ☐ Operates DC to above 1 MHz
- ☐ Binary-encoded for frequency selection



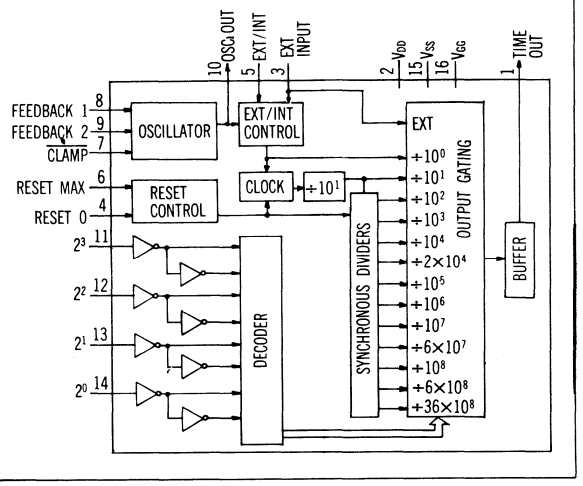
DESCRIPTION

The MK 5009 P is a highly versatile MOS oscillator and divider chain manufactured by Mostek using its depletion-load, ion-implantation process and P.-channel technology. The 16-pin DIP package provides frequency division ranges from 1 to 36×10^8. The circuit will operate from any of three frequency sources: the internal oscillator with an external RC combination; the internal oscillator with an external crystal; or with an externally-applied TTL signal. Control inputs provide additional versatility and allow the circuit to be used in a variety of applications including instruments, timers, and clocks.

With an input frequency of 1 MHz, the MK 5009 P provides the basic time periods necessary for most frequency measuring instruments, i.e., 1 μs through 100 seconds. One-minute, ten-minute, and one-hour periods are also available using a 1 MHz input. Using a 1/1.2 MHz input, the MK 5009 P can also provide a 50/60 Hz output for accurate generation of line frequencies in portable instruments or clocks.

The time-base output (TIME OUT) is a square wave, its frequency determined by the selected counter division, and by the oscillator frequency or external input. The falling edge of the output square wave should be used to control external gating circuitry.

FUNCTIONAL DIAGRAM



INDUSTRIAL

TIME OUT

ADDRESS INPUTS 2^3	2^2	2^1	2^0	WITHOUT RESET $R_{MAX}=0$ $R_O=0$	RESET Reset Max. $R_{MAX}=1$ $R_O=0$	RESET Reset Min. $R_{MAX}=0$ $R_O=1$	BYPASS MODES (see page 3) Mode 1 $R_{MAX}=V_{GG}$ $R_O=0$	Mode 2 $R_{MAX}=0$ $R_O=V_{GG}$	Mode 3 $R_{MAX}=V_{GG}$ $R_O=V_{GG}$
0	0	0	0	$\div 10^0$	$\div 10^0$	$\div 10^0$	$\div 10^0$	$\div 10^0$	$\div 10^0$
0	0	0	1	$\div 10^1$			$\div 10^1$	$\div 10^1$	$\div 10^1$
0	0	1	0	$\div 10^2$	Resets	Resets	$\div 10^2$	$\div 10^2$	$\div 10^2$
0	0	1	1	$\div 10^3$			$\div 10^3$	$\div 10^3$	$\div 10^3$
0	1	0	0	$\div 10^4$	Counters	Counters	$\div 10^4$	$\div 10^4$	$\div 10^4$
0	1	0	1	$\div 10^5$			$\div 10^2$	$\div 10^5$	$\div 10^2$
0	1	1	0	$\div 10^6$	to their	to their	$\div 10^3$	$\div 10^6$	$\div 10^3$
0	1	1	1	$\div 10^7$			$\div 10^4$	$\div 10^7$	$\div 10^4$
1	0	0	0	$\div 10^8$	Highest	Lowest	$\div 10^5$	$\div 10^5$	$\div 10^2$
1	0	0	1	$\div 6\times10^7$			$\div 6\times10^4$	$\div 6\times10^4$	$\div 6\times10^1$
1	0	1	0	$\div 36\times10^8$	States	States	$\div 36\times10^5$	$\div 36\times10^5$	$\div 36\times10^2$
1	0	1	1	$\div 6\times10^8$			$\div 6\times10^5$	$\div 6\times10^5$	$\div 6\times10^2$
	*			—			—	—	—
1	1	1	0	$\div 2\times10^4$			$\div 2\times10^1$	$\div 2\times10^1$	$\div 2\times10^1$
1	1	1	1	Ext. In.	Ext. In.	Ext. In.	Ext. Int.	Ext. Int.	Ext. Int.

*Addresses 1100 and 1101 result in Logic 0 at the output regardless of the state of the Reset Max. and Reset 0 inputs.

Logic 1 = High = V_{SS}

Logic 0 = Low = V_{DD}

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Terminal Relative to V_{SS} . . . . . + 0.3V to − 20V
Operating Temperature Range (Ambient) . . . . . 0°C to +70°C
Storage Temperature Range (Ambient) . . . . . − 55°C to + 150°C

RECOMMENDED OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{SS}	Supply Voltage	+ 4.5		+ 5.5	V	
V_{DD}	Supply Voltage	0.0		0.0	V	
V_{GG}	Supply Voltage	− 9.6		− 14.4	V	
f_{XTAL}	Crystal Frequency	0.1		2.0	MHz	
f_{RC}	RC Frequency	DC		200	kHz	
f_{EXT}	External Frequency	DC		2.0	MHz	
t_{PL}	Logic 0 Pulse Width, $\overline{\text{CLAMP}}$	—				Note 5
	Ext. Input	200			nsec	
t_{PH}	Logic 1 Pulse Width, Ext. Input	200			nsec	
	Reset Max	10.0			μsec	
	Reset 0	10.0			μsec	
R	Feedback Resistance	.01		2.5	MΩ	Fig. 1
V_{IL}	Input Voltage, Logic 0, Reset Inputs	0.0		0.8	V	
	Reset (Bypass Mode)	V_{GG}		V_{GG} + 1.0	V	Note 2
	All Other Logic Inputs			0.8	V	
V_{IH}	Input Voltage, Logic 1, All Logic Inputs	V_{SS}-1.0	V_{SS}	V_{SS} + 0.3	V	

ELECTRICAL CHARACTERISTICS

(V_{SS} = +5V ±10%; V_{DD} = 0 V; V_{GG} = −12.0 V ±20%; 0° C ≤ T_A ≤ 70° C)

	PARAMETER	MIN	TYP†	MAX	UNITS	NOTES
I_{SS}	Supply Current, V_{SS}		6.0	11.0	mA	Note 1
I_{GG}	Supply Current, V_{GG}		6.0	11.0	mA	
I_{IL}	Input Current, Logic 0			− 1.6	mA	Note 2; V_I = 0.4V
V_{OL}	Output Voltage, Logic 0			0.4	V	I_{OL} = 1.6mA*
V_{OH}	Output Voltage, Logic 1	2.4			V	I_{OH} = −40μA*
f_{STA}	Frequency Stability w/ Volt. Change, RC Mode		± 3.0		%/V	Note 3
	/ Temp. Change, RC Mode		− 0.2		%/°C	
	Crystal Mode		—			Note 4
$t_{e\text{-}e}$	Jitter, Edge-to-Edge Variation		<15		nsec	Temp. & Supply Voltage Constant

†Typical values at V_{SS} = +5V, V_{DD} = 0V, V_{GG} = −12V, and T_A = 25°C

1. Logic inputs at V_{SS}, output open circuited. Each logic input (see Note 2) contributes an additional 1.6 mA (max.) to I_{SS} when at logic 0.
2. Logic Inputs are: Reset Max; Reset 0; Address Inputs; Ext. Input; Ext/Int Select; and $\overline{\text{Clamp}}$.
3. Frequency variations due to power supply changes only.
4. Crystal mode stability is dependent upon crystal.
5. Minimum logic 0 time at clamp input is 50% of oscillator period.

*V_{OH}, V_{OL} apply only to Time Out.

INDUSTRIAL

DESCRIPTION OF OPERATION

The MK 5009 P consists basically of a series of counters, selectable via an internal multiplexer. The $\div 10^1$ counter output is used to generate an internal clock signal for the 10^2 through 36×10^8 counter stages, which are fully synchronous with each other.

OSCILLATOR CONTROLS

Operation in the RC oscillator mode is achieved as shown in Figure 1. Frequency, f, is approximately 0.8/RC. The clamp circuit can be used in the RC mode to provide one-shot or accurate start-up operations. When Clamp goes to a logic 0, the internal circuitry is held at a reference level so that upon release of the Clamp (return to logic 1), the oscillator's first cycle will be a full cycle.

The crystal oscillator mode is shown in Figure 2. Values for the resistors are chosen to bias the internal circuitry for optimum performance. The two capacitors are chosen to provide the loading capacitance (C_L) specified for the selected crystal. It is recommended that C1 = C2 = 2 C_L.

RESET/BYPASS CONTROLS

The MK 5009 P provides two different reset conditions. A positive-going pulse of 10 μs or longer on Reset 0 will reset counters to their lowest state, while a positive-going pulse at Reset Max will reset counters to their highest state. The Reset Max control enables the user to set up the counters to provide a falling edge at the next oscillator cycle or negative-going external input, regardless of which divider chain is selected.

In addition, taking one or both Reset Inputs to the most negative voltage, V_{GG}, allows bypassing portions of the divider chain for testing or other purposes (see table on page 1).

EXTERNAL/INTERNAL FREQUENCY SOURCE

When using an external signal source to operate the MK 5009 P, that signal should be applied at the External Input (Pin 3), and the External/Internal Select (Pin 5) should be brought to logic 1.

For operation with an internal signal, the External/Internal Select should be at logic 0.

OSCILLATOR OUTPUT

The oscillator output, provided at Pin 10, is not a true logic output, but may be used to drive a high impedance device such as a junction FET or other MOS circuitry.

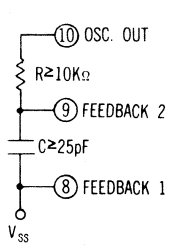


FIG. 1

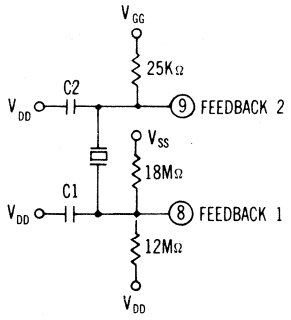
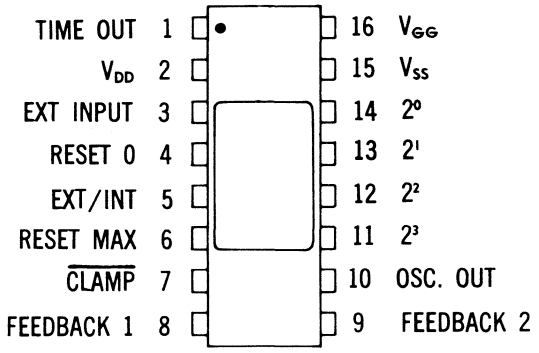
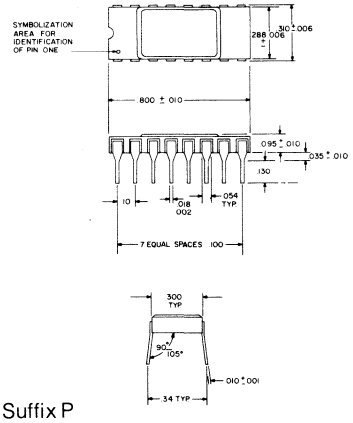


FIG. 2

PIN CONNECTIONS

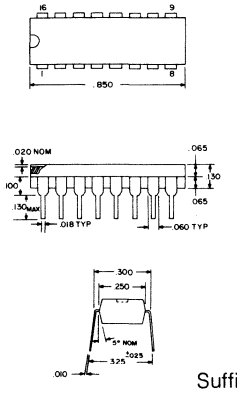


PACKAGE
16-pin ceramic dual-in-line



Suffix P

PACKAGE
16-pin plastic dual-in-line



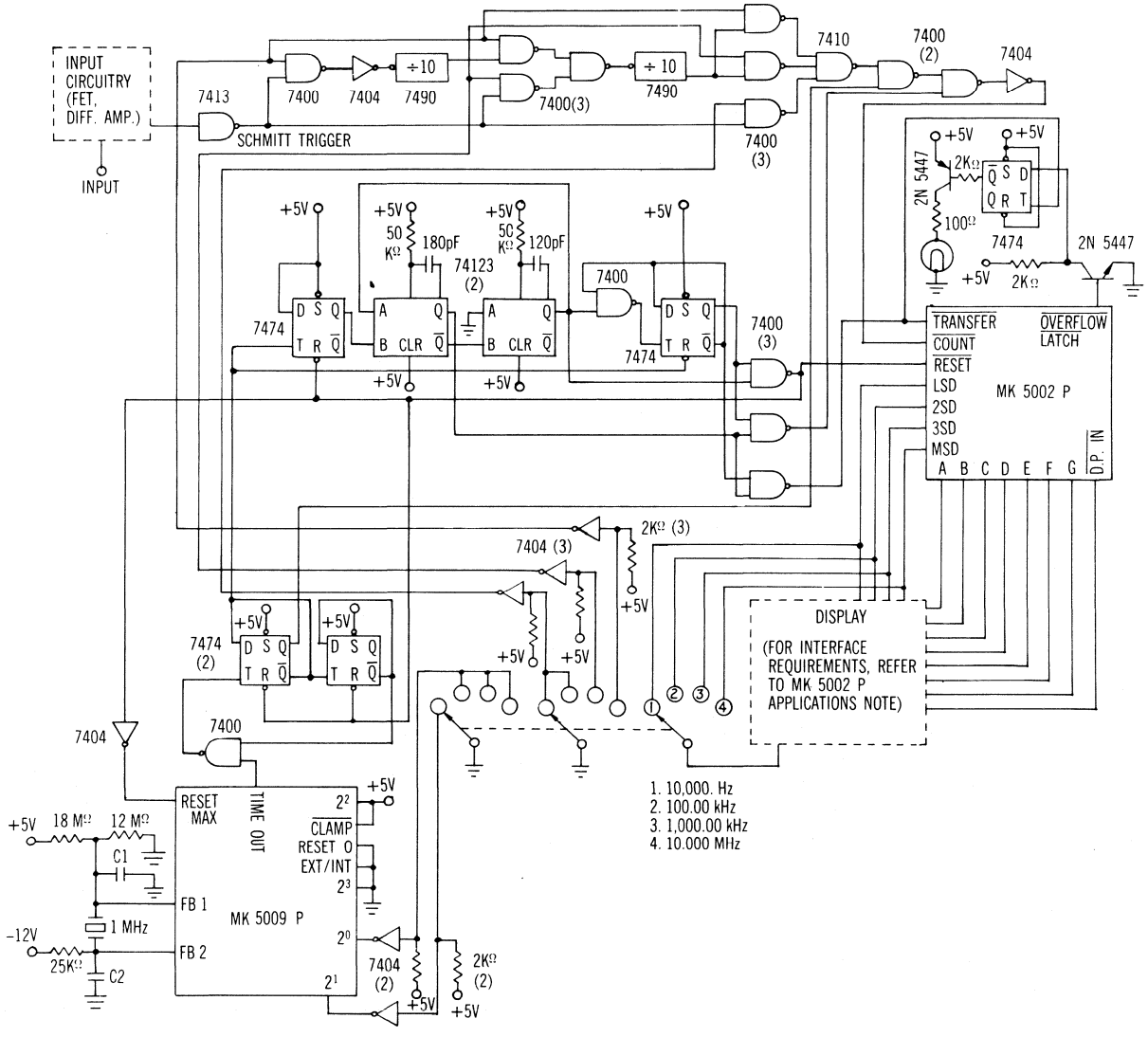
Suffix N

INDUSTRIAL

APPLICATION — 10 MHz Frequency Counter

The circuit shown below is a frequency counter capable of counting input rates up to 10 MHz, selected in four ranges. The MK 5009 P provides the time base intervals while the Mostek MK 5002 P counter circuit provides counting, storage, and display functions. Two decades of prescaling using TTL are employed. TTL one-shots provide proper timing for the 5002.

To replace the functions of the MK 5009 P, an active device and Schmitt trigger for the crystal oscillator would be needed, plus six 7490's to achieve the correct time out. Replacing the functions of the MK 5002 would require four 7490's, four 7475's, and four BCD-to-seven-segment decoders.



MK 50240/1/2P
MK 50240/1/2N

MOS Top Octave Frequency Generator

MOSTEK®

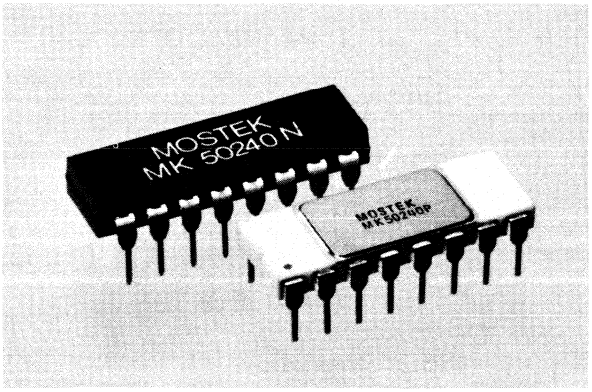
FEATURES

- ☐ Single Power supply
- ☐ Broad supply voltage operating range
- ☐ Low power dissipation
- ☐ High output drive capability

MK 50240 — 50% Output Duty Cycle

MK 50241 — 30% Output Duty Cycle

MK 50242 — 50% Output Duty Cycle



DESCRIPTION

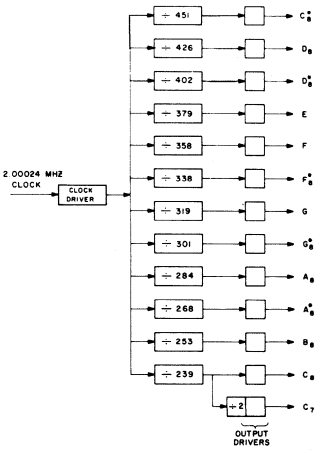
The MK 50240 is one of a family of ion-implanted, P-channel MOS, synchronous frequency dividers.

Each output frequency is related to the others by a multiple $12\sqrt{2}$ providing a full octave plus one note on the equal tempered scale.

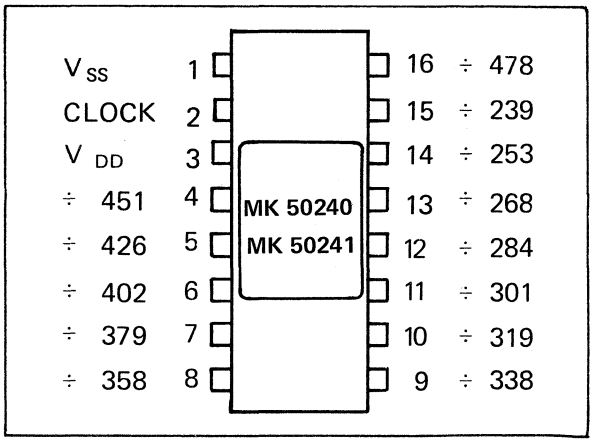
Low threshold voltage enhancement-mode, as well as depletion mode devices, are fabricated on the same chip allowing the MK 50240 family to operate from a single, wide tolerance supply. Depletion-mode technology also allows the entire circuit to operate on less than 600 mW of power. The circuits are packaged in 16-pin ceramic dual-in-line packages.

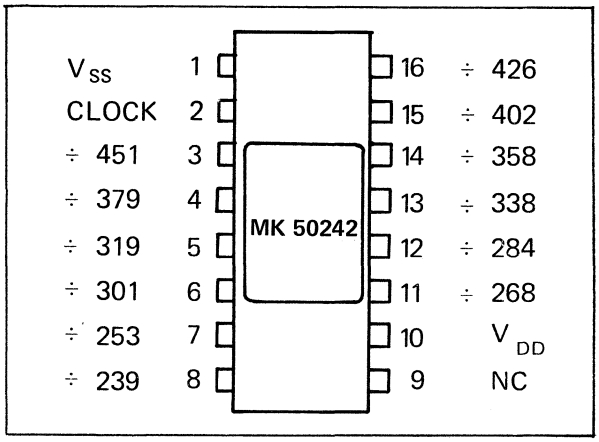
RFI emination and feed-through is minimized by placing the input clock between the V_{DD} and V_{SS} pins. Internally the layout of the chip isolates the output buffer circuitry from the divisor circuit clock lines. Also, the output buffers limit the minimum rise-time under no load conditions to reduce the R.F. harmonic content of each output signal.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS





INDUSTRIAL

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} ..... +0.3V to −20V

Operating Temperature (Ambient)..... 0°C to 50°C

Storage Temperature (Ambient)..... −40°C to 100°C

RECOMMENDED OPERATING CONDITIONS

($0°C \leq T_A \leq 50°C$)

	PARAMETER	MIN	TYP	MAX	UNITS	FIGURE
V_{SS}	Supply Voltage	0		0	V	
V_{DD}	Supply Voltage	−11.0	−15.0	−16.0	V	

ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 50°C$; V_{SS} = 0, V_{DD} = −11 to −16V unless otherwise specified)

	PARAMETER	MIN	TYP	MAX	UNITS	FIGURE
V_{IL}	Input Clock, Low	0		−1.0	V	FIG. 1
V_{IH}	Input Clock, High	V_{DD} + 1.0		V_{DD}	V	
f_I	Input Clock Frequency	100	2000.240	2500	kHz	
t_r , t_f	Input Clock Rise & Fall Times 10% to 90% @ 2.5 MHz			30	nsec	FIG 1
t_{on} , t_{off}	Input Clock On and Off Times @ 2.5 MHz		200		nsec	FIG. 1
C_I	Input Capacitance		5	10	pF	
V_{OH}	Output, High @ .70 mA	V_{DD} + 1.5		V_{DD}	V	FIG. 2
V_{OL}	Output, Low @ .75 mA	V_{SS} − 1.0		V_{SS}	V	FIG. 2
t_{ro}, t_{fo}	Output Rise & Fall Times, 500 pF Load	250		2500	nsec	FIG. 3
t_{on}, t_{off}	Output Duty Cycle MK 50240P & MK 50242P MK 50241P (Pin 16 50%)		50 30		% %	
I_{DD}	Supply Current		24	37	mA	outputs unloaded

INDUSTRIAL

FIGURE 1
INPUT CLOCK WAVEFORM

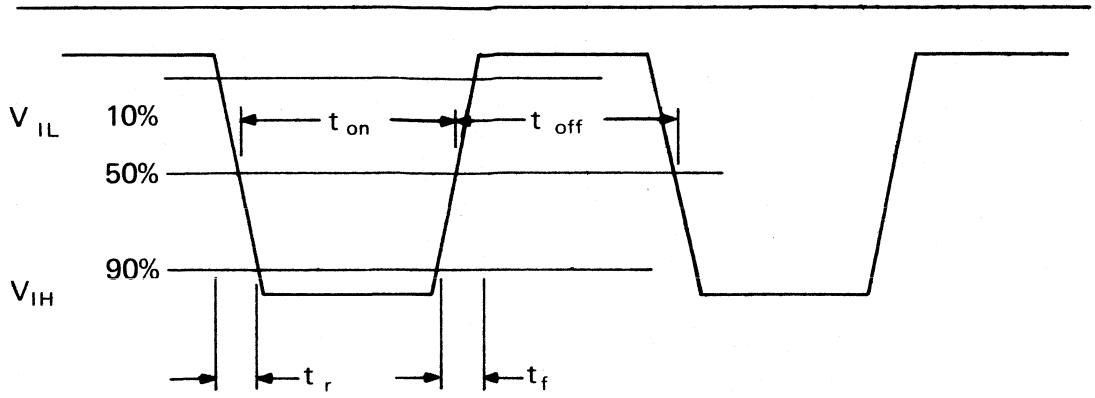
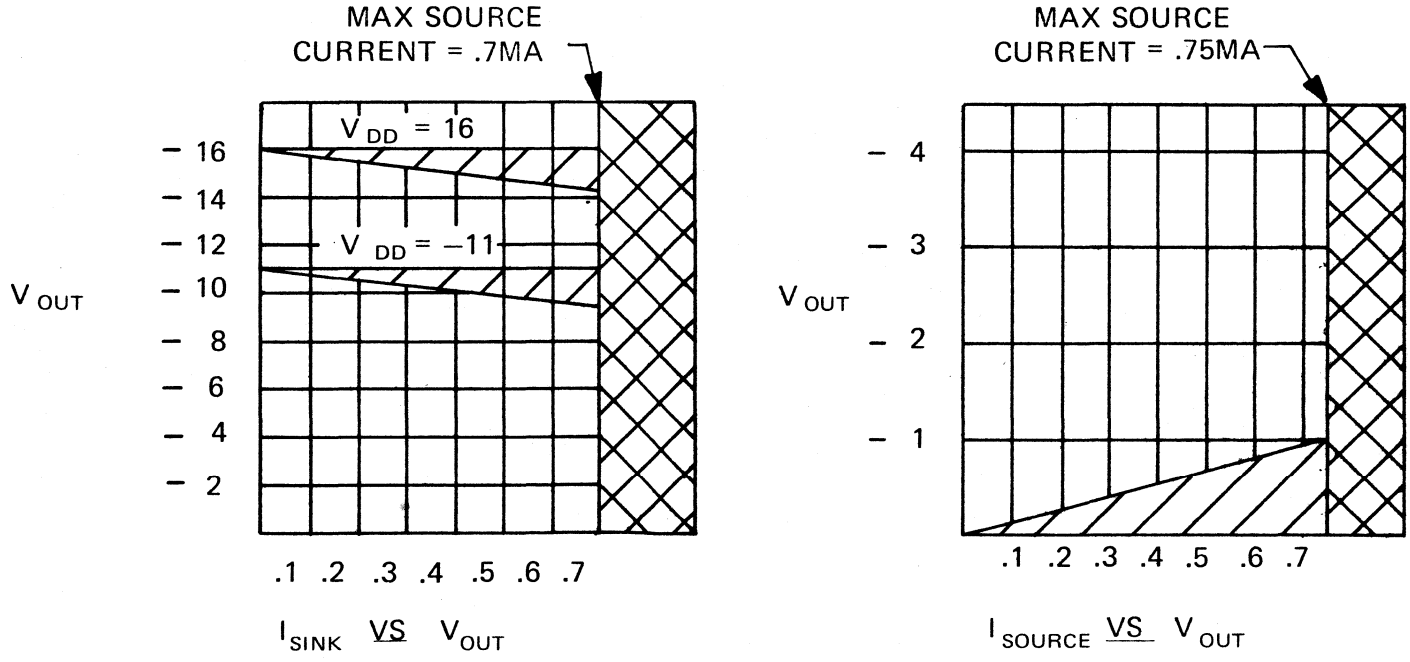


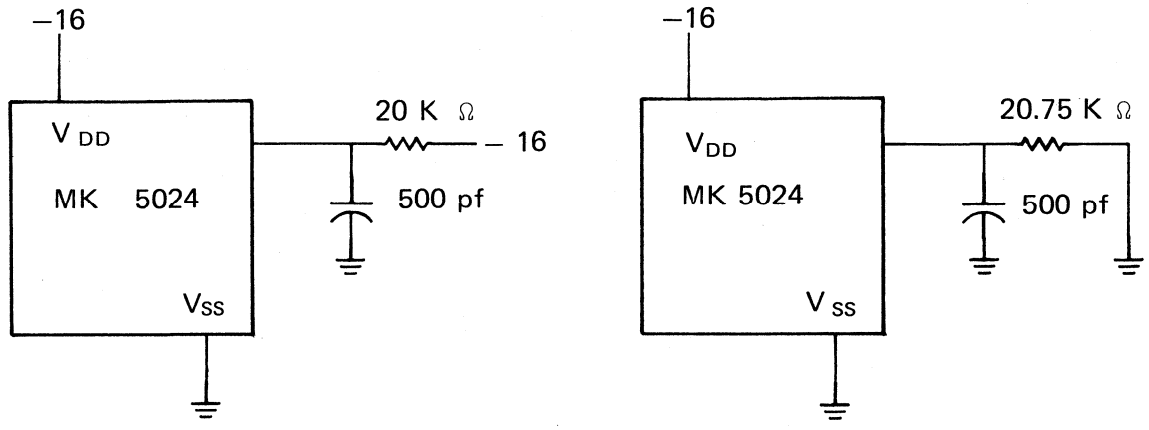
FIGURE 2
OUTPUT SIGNAL D. C. LOADING



SINK CURRENT TO CHIP V_{DD} — (OPERATING AREA)

SINK CURRENT FROM CHIP V_{SS} — (CURRENT OVERLOAD AREA)

FIGURE 3
OUTPUT LOADING

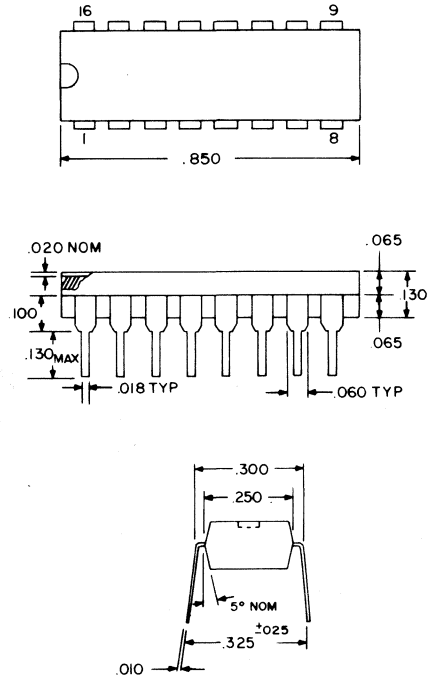


t_{fo} Test

t_{ro} Test

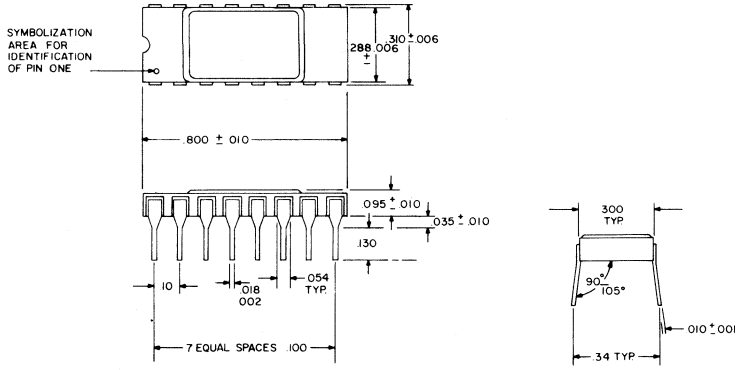
PHYSICAL DESCRIPTION

16–lead plastic dual-in-line hermetic package



Suffix N

16–lead side brazed ceramic dual-in-line hermetic package



Suffix P

NOTE:

A. Pin 1 indicated by index dot
B. All dimensions in inches

PRELIMINARY

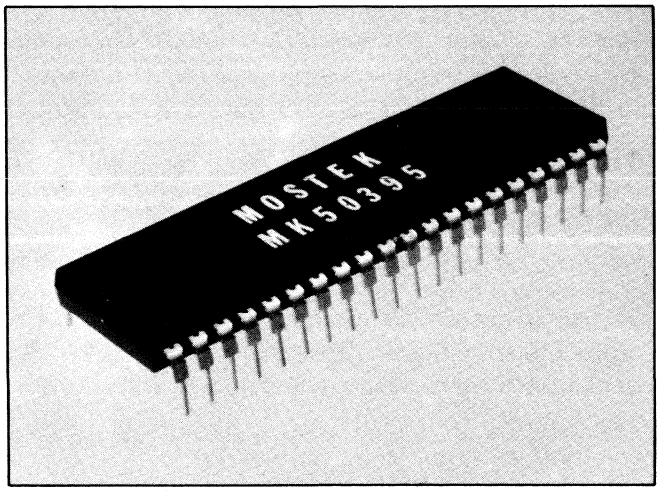
MK50395N

MOS Six-Decade Counter / Display Decoder

MOSTEK

FEATURES:

- ☐ Single power supply
- ☐ Schmitt-Trigger on the count-input
- ☐ Six decades of synchronous up/down counting
- ☐ Look-ahead carry or borrow
- ☐ Loadable counter
- ☐ Loadable compare-register with comparator output
- ☐ Multiplexed BCD and seven-segment outputs
- ☐ Internal scan oscillator
- ☐ Direct LED segment drive
- ☐ Interfaces directly with CMOS logic
- ☐ Leading zero blanking



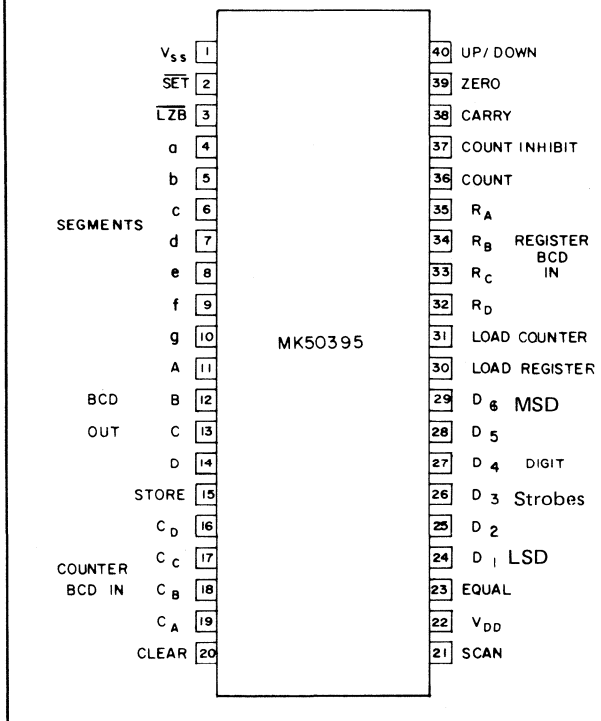
INDUSTRIAL

DESCRIPTION:

The MK 50395 is an ion-implanted, P-channel MOS six-decade synchronous up/down-counter/display driver with compare-register and storage-latches. The counter as well as the register can be loaded digit-by-digit with BCD data. The counter has an asynchronous-clear function.

Scanning is controlled by the scan oscillator input which is self-oscillating or can be overdriven by an external signal. The six-decade-register is constantly compared to the state of the six-decade-counter and when both the register and the counter have the same content, an EQUAL signal is generated. The contents of the counter can be transferred into the 6-digit latch which is then multiplexed from MSD to LSD in BCD and 7-segment format to the output. The seven-segment decoder incorporates a leading-zero blanking circuit which can be disabled by an external signal. This device is intended to interface directly with the standard CMOS logic families.

PIN CONNECTION



OPERATIONS:

SIX DECADE COUNTER, LATCH

The six decade counter is synchronously incremented or decremented on the positive edge of the count input signal. A Schmitt trigger on this input provides hysteresis for protection against both a noisy environment and double triggering due to a slow rising edge at the count input.

The count inhibit can be changed in coincidence with the positive transition of the count input; the count input is inhibited when the count inhibit is high.

The counter will increment when up/down input is high (V_{SS}) and will decrement when up/down input is low. The up/down input can be changed .75 μs prior to the positive transition of the count input.

The clear input is asynchronous and will reset all decades to zero when brought high but does not affect the six digit latch or the scan counter.

As long as store input is low, data is continuously transferred from the counter to the display. Data in the counter will be latched and displayed when store input is high. Store can be changed in coincidence with the positive transition of the count input.

The counter is loaded with BCD data, digit by digit corresponding to the digit strobe outputs. BCD thumbwheel switches with four diodes per decade connected between the digit strobe outputs and the BCD inputs will load the counter when the load counter input is taken high. Counter input is inhibited while the load counter input is high. The load counter input must remain high a minimum of six digit strobe output periods.

Three basic outputs originate from the counter: zero output, equal output, and carry output. Each output goes high on the positive (V_{SS}) going edge of the count input under the following conditions:

Zero output goes high for one count period when all decades contain zero. During a load counter operation the zero output is inhibited.

Equal output goes high for one count period when the contents of the counter and compare register are equal. The equal output is inhibited by a load counter or load register operation.

The carry output goes high with the leading ege of the count input at the count of 000000 when counting up or at 999999 when counting down and goes low with the negative going edge of the same count inpulse.

A count frequency of 1 MHz can be achieved if the equal output, zero output and carry output are not used. These outputs do not respond at this frequency due to their output delay illustrated on the timing diagram.

SIX DECADE COMPARE REGISTER

The register is loaded with BCD data digit-by-digit corresponding to the digit strobe outputs. BCD thumbwheel switches with four diodes per decade connected between the digit strobe outputs and the BCD inputs will load the register when the load register input is taken high. The load register input must remain high a minimum of six digit strobe output periods.

This register is a static register and will not be cleared by the clear input.

BCD & SEVEN SEGMENT OUTPUT

BCD or seven segment outputs are available. Digit strobes are decoded internally by a divide by six Johnson counter. This counter scans from MSD to LSD. By bringing the $\overline{SET}$ input low, this counter will be forced to the MSD decade count. During this time the segment outputs are blanked to protect against display burn out.

Both the segment outputs and digit strobes are blanked during the interdigit blanking time. Leading zero blanking effects only the segment outputs. This option is disabled by bringing the $\overline{LZB}$ input high.

BCD output data changes at the beginning of the interdigit blanking time. These outputs are CMOS compatible.

SCAN OSCILLATOR

The MK 50395 has an internal oscillator. The frequency of the scan oscillator is determined by an external capacitor between V_{SS} and scan input. The wave form present on the scan oscillator input is triangular.

An external scan oscillator may also be used to drive the scan input. In either case, external capacitors of 150 pF each will be required from V_{SS} to Counter BCD inputs and register BCD inputs. This will allow asynchronous loading of the BCD inputs.

If external capacitors on the BCD inputs are undesirable, it will be necessary to synchronize the negative going edge of the load register and/or load counter command to coincide with the positive going edge of the scan input signal. Also the V_{SS} range should be limited from 10.8 to 13.2 volts.

Typically, the scan oscillator will oscillate at the following frequencies with these nominal capacitor valves from V_{SS} to scan input.

	Min	Max
820 pF	1.4 KHz	4.8 KHz
470 pF	2.0 KHz	6.8 KHz
120 pF	7.0 KHz	20 KHz

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Terminal Relative to V_{SS} . . . . . +0.3V to −20V
Operating Temperature Range (Ambient) . . . . . 0°C to +70°C
Storage Temperature Range (Ambient) . . . . . 0°C to +100°C

MAXIMUM OPERATING CONDITIONS

	PARAMETER	MIN	MAX	UNITS	NOTES
T_A	Operating Temperature	0	70	C	
V_{SS}	Supply Voltage (V_{DD} = 0V)	10	15	V	10
I_{SS}	Supply Current		40	mA	4
B_V	Break Down Voltage (Segment only @ 10 μA)		V_{SS} − 26	V	

ELECTRICAL CHARACTERISTICS

(V_{DD} = 0V, V_{SS} = + 10.0V to + 15.0, 0°C ≤ T_A ≤ 70°C)

Static Operating Conditions

	PARAMETER	MIN	MAX	UNITS	NOTES
V_{IL}	Input Low Voltage, "0"	V_{DD}	$0.2V_{SS}$	V	
V_{IH}	Input High Voltage, "1"	V_{SS}−1	V_{SS}	V	1
V_{OL}	Output Voltage "0" @ 30μA		$0.2V_{SS}$	V	3
V_{OH}	Output Voltage "1" @ 1.5 mA	$0.8V_{SS}$		V	3
I_{OH}	Output Current "1" digit strobes segment outputs	 3.0 10.0		 mA mA	 6 2
I_{SCAN}	Scan Input Pullup Current @ 0V		5.5	mA	
I_{SCAN}	Scan Input Pulldown Current @ 15V	2	40	μA	
$I_{\overline{SET}}$	$\overline{SET}$ Input Pullup Current @ 0V	5	60	μA	

INDUSTRIAL

Dynamic Operating Conditions

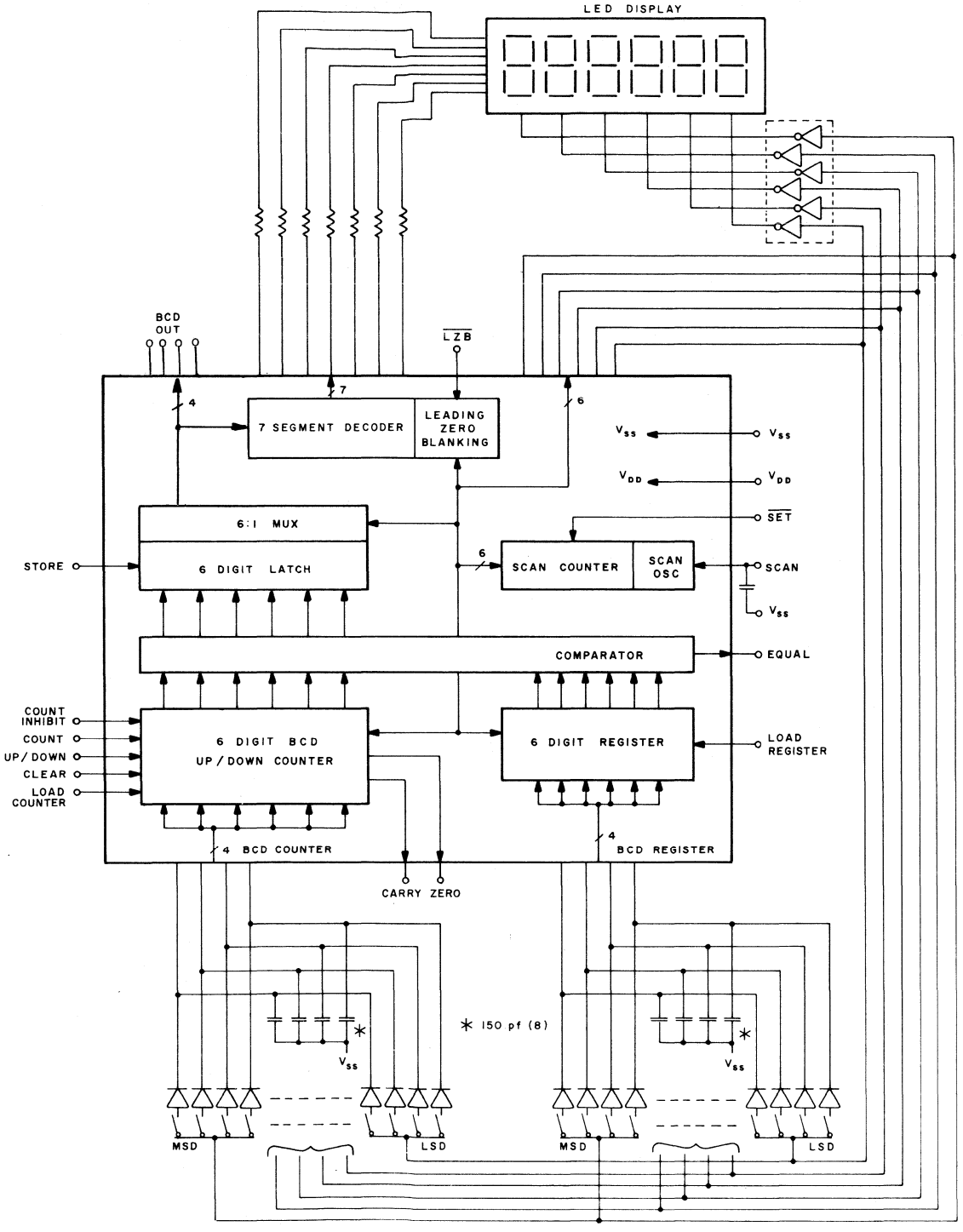
	PARAMETER	MIN	MAX	UNITS	NOTES
f_{CI}	Count Input Frequency	0	1.00	MHz	5, 9
f_{SI}	Scan Input Frequency	0	20	KHz	
t_{CPW}	Count Pulse Width	400		ns	11
t_{SPW}	Store Pulse Width	2.0		μs	
t_{SS}	Store Setup Time	0		μs	7
t_{CIS}	Count Inhibit Setup Time	0		μs	7
t_{UDS}	Up/Down Setup Time	−.75		μs	7
t_{CPW}	Clear Pulse Width	2.0		μs	7
t_{CS}	Clear Setup Time	0.5		μs	7
t_{OA}	Zero Access Time		3.0	μs	7
t_{OH}	Zero Hold Time		1.5	μs	7
t_{CA}	Carry Access Time		1.5	μs	7
t_{CH}	Carry Hold Time		0.9	μs	8
t_{EA}	Equal Access Time		2.0	μs	7
t_{EH}	Equal Hold Time		1.5	μs	7
t_L	Load Time	$1/6\ f_{SI}$			

NOTES:

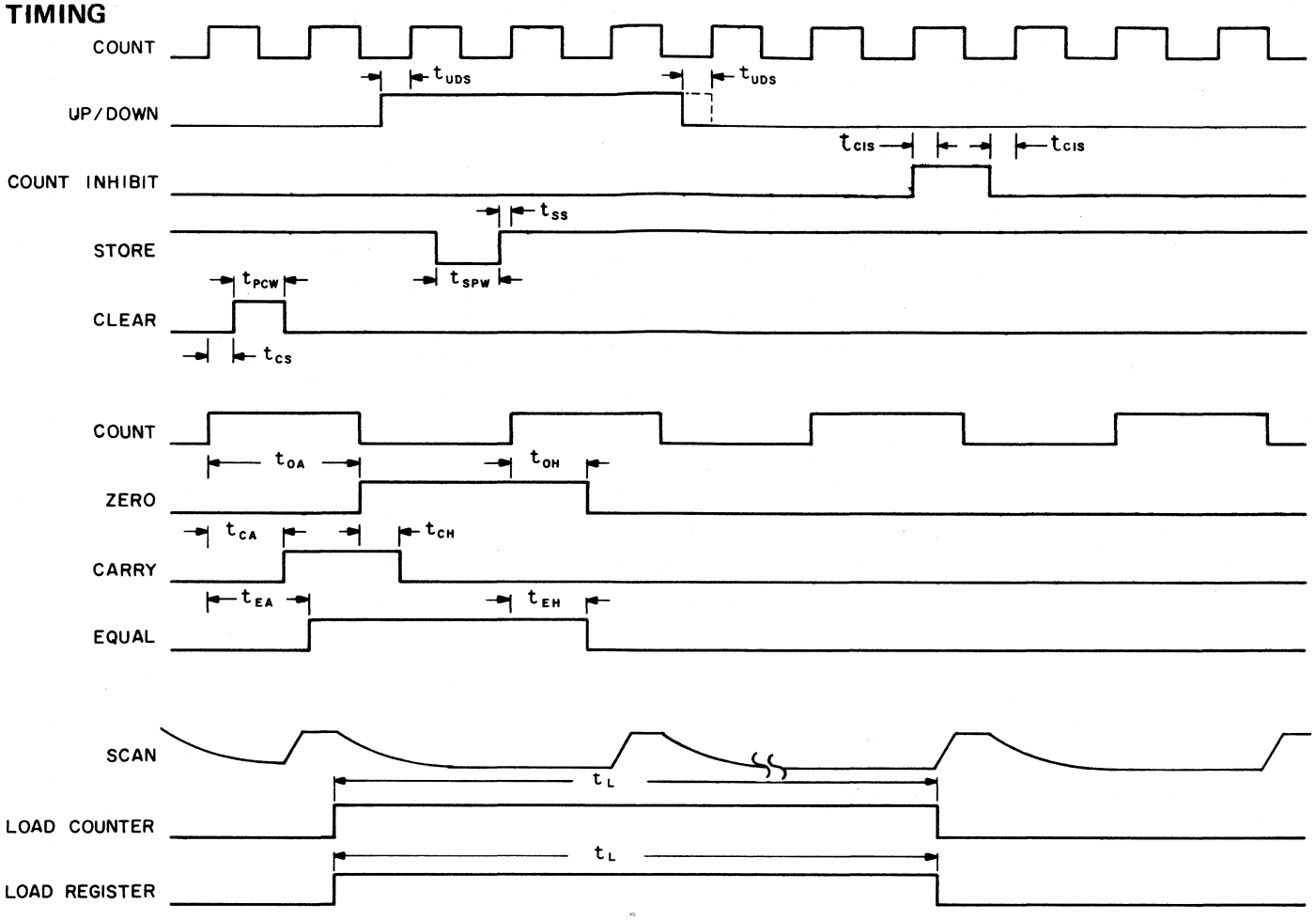
1. MIN V_{IH} for R_A R_B R_C R_D C_A C_B C_C C_D inputs is V_{ss} − 2.5V These inputs have internal pulldown resistors to V_{DD}
2. For $V_{OUT} = V_{ss} - 3.0$ volts
3. This applies to the push pull CMOS compatible outputs. Does not include digit strobes or segment outputs.
4. I_{DD} with inputs and outputs open. This does not include segment current. Total power per segment must be limited not to exceed power dissipation of package. ($\Theta_{JA} = 100\ ^{\circ}C/Watt$)
5. Measured at 50% duty cycle.
6. For $V_{OUT} = V_{ss} - 2.0$ volts.
7. The positive edge of the count input is the t = 0 reference
8. Measured from negative edge of count input
9. If carry, equal, or zero outputs are used the count frequency will be limited by their respective output times.
10. With 150 pF capacitor to V_{ss} from counter BCD and register BCD inputs.
11. The count pulse width must be greater then the carry access; time when using the carry output.

INDUSTRIAL

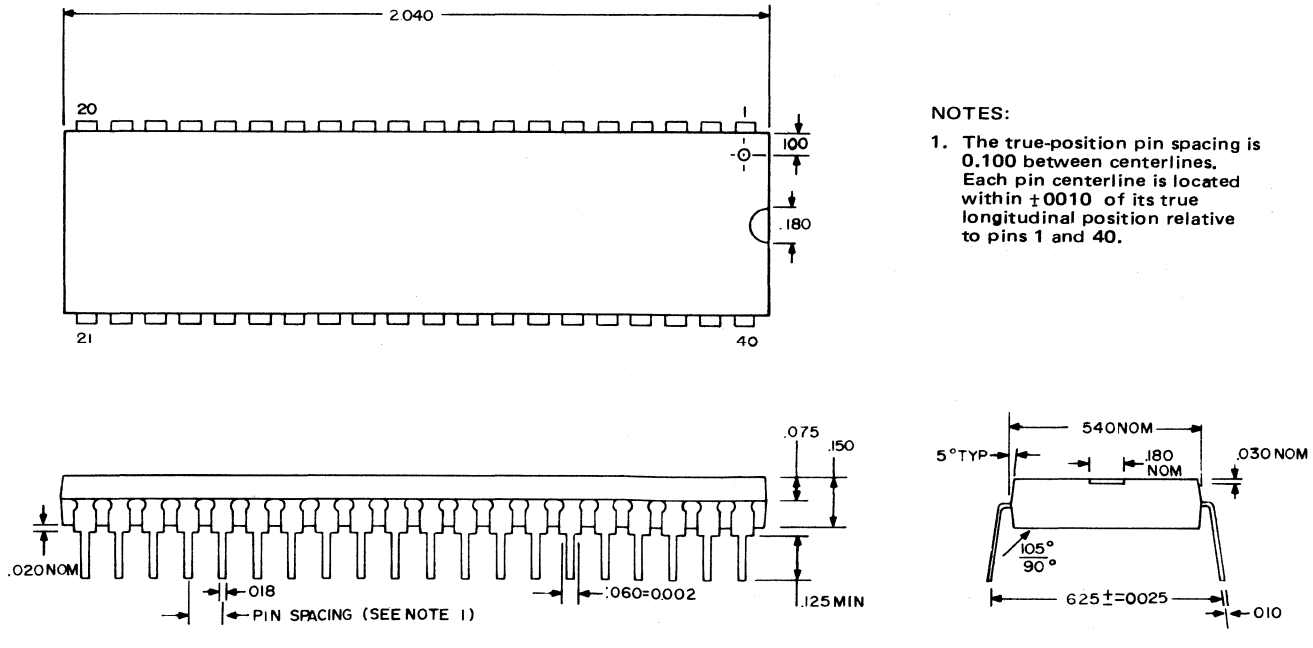
FUNCTIONAL DIAGRAM



TIMING



PACKAGE DESCRIPTION - 40-Pin Dual-in-Line Plastic Package



NOTES:

1. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0010 of its true longitudinal position relative to pins 1 and 40.

MEMORIES

MICRO-
PROCESSORS

CONSUMER
CIRCUITS

INDUSTRIAL

FUTURE
PRODUCTS

MOSTEK

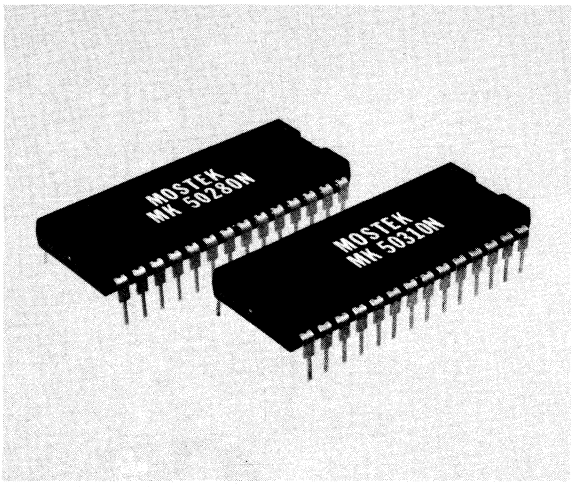
PRELIMINARY

MK 50280N Series
MK 50310N Series

8-Digit Calculator Series MOSTEK®

FEATURES:

- ☐ Single power supply with wide tolerances
- ☐ Operation directly from a nine volt battery (Applies to –1 parts only)
- ☐ Low power consumption
- ☐ Direct segment drive for LED displays
- ☐ Segment current regulated by a single resistor
- ☐ Fluorescent display compatible (Applies to –3 parts only)
- ☐ Internal clock requiring no external components
- ☐ Internal encoding of keyboard inputs
- ☐ Internal debouncing of keyboard inputs
- ☐ Internal power up clear requiring no external components



CALCULATOR PRODUCTS

MK 50282–8 digit, five-function (+, –, X, ÷, %) with average, repeat add/subtract, automatic constant, and percentage add on/discount

MK 50314 – 8 digit, five-function (+, –, ÷, %) five key memory calculator (M+, M-, MR, MC, MX) with repeat add/subtract, automatic constant and percentage add on/discount

MK50101N
MK50102N
MK50075N

Financial
Calculator Chip Set

MOSTEK

DESCRIPTION:

The MK 50075, ALU circuit combined with the MK 50101, MK 50102 ROM circuits forms a nine or twelve digit algebraic business calculator. The calculator normally has a nine digit display although all internal calculations are computed to thirteen digits. By adding two diodes and a switch twelve digits can be displayed. The display format may be fixed point (user programmed) or floating point.

The chip set has nine memory registers. The memory operations of addition and subtraction are performed on the contents of memory register one and the display register without affecting the display contents.

The calculator has the standard four functions of addition, subtraction, multiplication, and divisions. The equal key serves two functions. The first time it is pressed, it completes the previously entered operation. The second time it is pressed the calculator will perform constant operations in which the second numerical entry is treated as the constant. The calculator also performs the functions of percent, y^x, and gross profit margin.

Stored in its ROM's this chip set has a unique financial program. Tied in with this program are five financial keys: i, interest; n, number of payments; PMT, amount of payment; PV, present value; and FV, future value. All financial calculations require a minimum of three input parameters to solve for the other two. Input parameters may be entered in any order from the keyboard or be stored in the financial registers as the result of pervious calculations. These keys make financial calculations easier than adding or subtracting.

KEYBOARDS

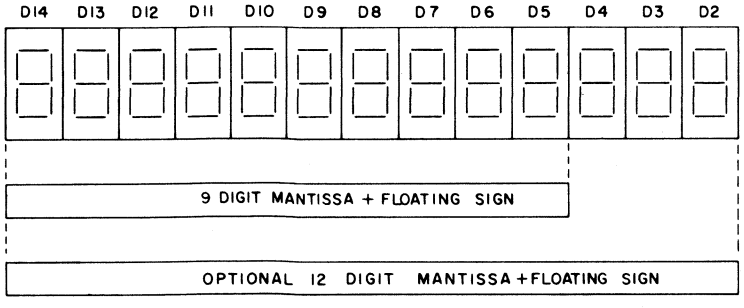
y^x	%	GPM	DSP	C/CE
n	i	PMT	PV	FV
M+	M−	RCL	EX	CM
7	8	9	÷	
4	5	6	X	
1	2	3	−	
0	.	=	+	

Financial Calculator with One Memory Register

y^x	%	GPM	DSP	C/CE
n	i	PMT	PV	FV
M+ (1)	M− (1)	STO (x)	RCL (x)	EXM (x)
7	8	9	÷	
4	5	6	X	
1	2	3	−	
0	.	=	+	

Financial Calculator with Nine Memory Registers

DISPLAY FORMAT & CONNECTIONS



CONSUMER CIRCUITS

MK50103N
MK50104N
MK50075N

Scientific
Calculator Chip Set

MOSTEK

DESCRIPTION:

The MK 50075, ALU circuit combined with the MK 50103, 50104 ROM circuits forms a powerful twelve digit scientific calculator. The display format can be fixed point (user programmed) or floating point in either business or scientific notation. The calculator has four rotatable stack registers plus nine addressable memory registers. All entries use the reverse polish notation.

Effective combination of key functions on this calculator make it possible to offer fifty-five functions with thirty keys. Multifunction keys are accomplished by utilizing the SHFT/DSP, INV/STO, and HYP/RCL control keys. SHFT (Function)enables the upper case key function while INV (Function) enables the inverse of a function. The HYP key is used in conjunction with hyperbolic functions. Several keys have both upper case, and inverse functions while COS, SIN, and, TAN have hyperbolic upper case, and inverse functions. The order in which the control keys are entered will have no effect on the function. For example, both the key sequence SHFT, INV, C→F and INV, SHFT, C→F will convert degrees Fahrenheit into degrees celsius.

The calculator can work trigonometric functions in either degrees, grads, or radians. When in the radian mode an indicator is turned on. Switching between grads and degrees is achieved by a slide switch while switching from grads to radians or degrees to radians is a key function. The calculator can do the following transcendental functions: sinx, arcsinx, cosx, arccosx, tanx, arctanx, sinhx, arcsinhx, coshx, arccoshx, tanhx, arctanhx, e^x, lnx, 10^x, and logx.

Besides trancendentals it calculates the single variable functions of X!, 1/X, $\sqrt{X}$, and x^2 and the two variable functions of y^x, $\sqrt[x]{y}$, %, and Δ%. It has ten preprogramed conversions which automatically change the contents of the display register into the desired units. It calculates mean and standard deviation using the unbiased method. Its Σ+, Σ −, and RCL Σ+ functions combined with its polar to rectangular conversion makes vector addition straight forward.

Functions available on Scientific Calculator:

Clear
Clear display
Add, subtract, multiply, divide

Scientific display format; 10-digit mantissa, 2-digit exponent, floating decimal
Mode set to radians
Fix decimal point (0-9) in display
Sine
Cosine
Tangent
Hyperbolic sine
Hyperbolic cosine
Hyperbolic tangent

Memory store, 9 registers
Memory recall, 9 registers
Memory exchange, 9 registers
X ⟷ Y exchange

Common Log
Natural log

4-stack register
Rotate stack
Recall last X

Y to the X power
Reciprocal for all values exponent range from +99 through −100
PI
Change sign
Square root
Factorials

Summation plus (adds X and Y to memory for vector addition; recalls sum of X and sum of Y)
Percentage
Percentage difference (Δ%)

Mean
Standard deviation

Centigrade to fahrenheit
Liters to gallons
Centimeters to inches
Kilograms to pounds
Degrees to radians
Set radian mode for trigonometric functions
Trigonometric rectangular to polar
Hyperbolic rectangular to polar

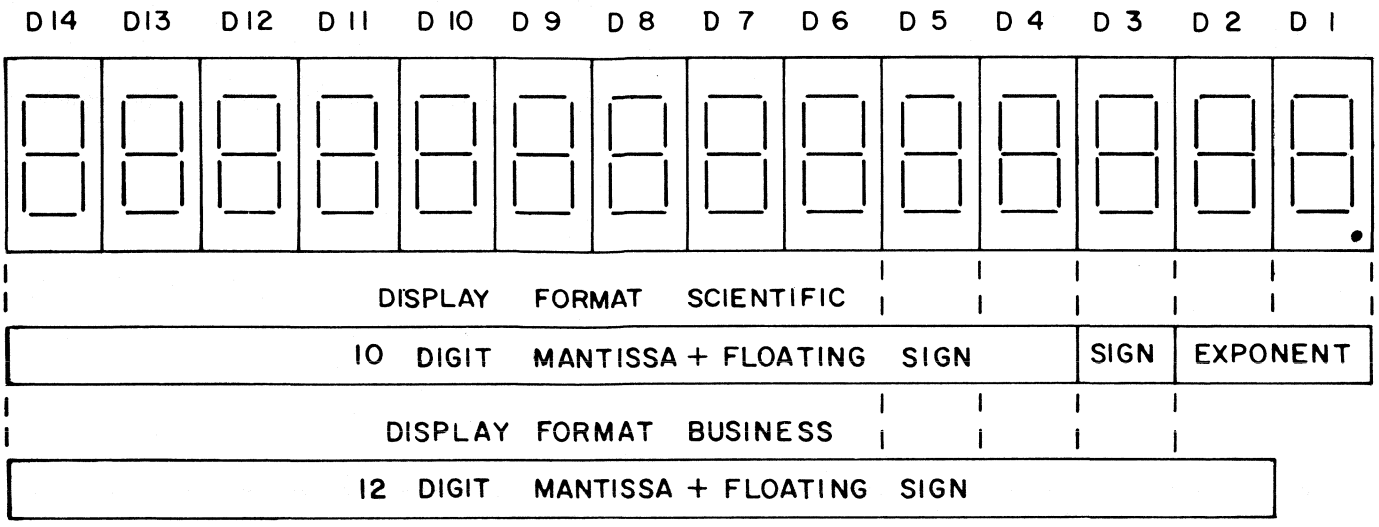
These functions are obtainable through the INVERSE calculation sequence:

Business display format, 12-digits, floating decimal point
Arc sine
Arc cosine
Arc tangent
Arc hyperbolic sine
Arc hyperbolic cosine
Arc hyperbolic tangent
Xth root of Y
Gross profit margin percentage
Summation minus for vector subtraction

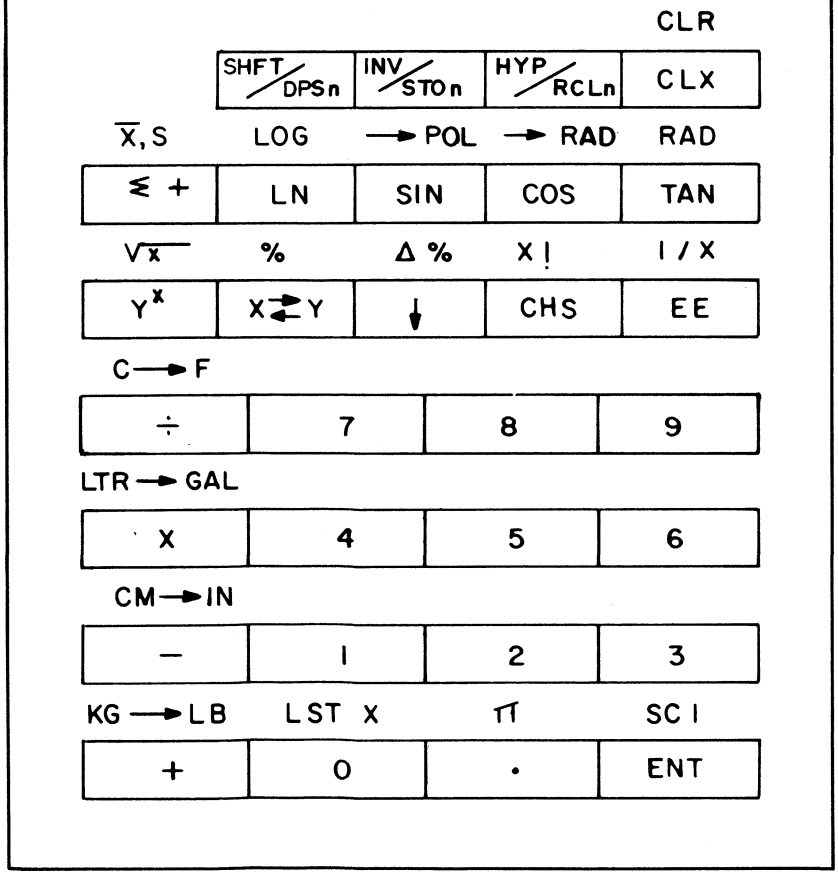
Anti log, natural (e^x) for all values from +230 through −230
Anti log, common (10^x), for all values from +99.9 through −99.9
Trigonometric polar to rectangular
Hyperbolic polar to rectangular
Set degree mode for trigonometric functions
x^2
Fahrenheit to centigrade
Gallons to liters
Inches to centimeters
Pounds to kilograms

CONSUMER CIRCUITS

DISPLAY FORMAT & CONNECTIONS



KEYBOARD



PRELIMINARY

MK 50250N Series

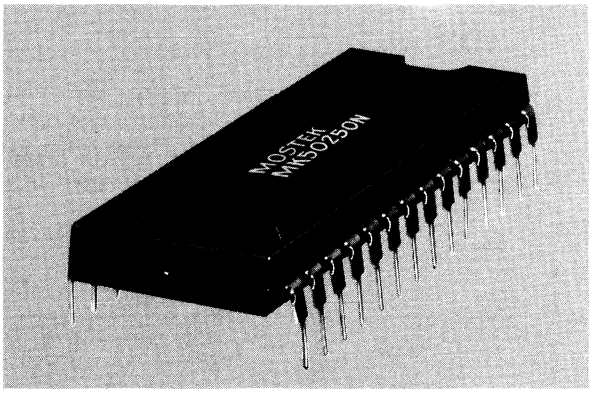
MOS Digital Alarm Clock

MOSTEK

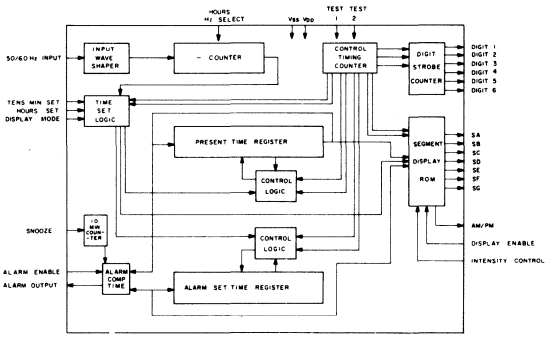
FEATURES

Single Voltage Power Supply
Intensity Control
Simple Time Setting
4 or 6 Digit Display
AM/PM and Activity Indicator
Selectable Input Frequency and Output Mode
- MK 50250 – 12 hr/60 Hz or 24 hr/50 Hz
- MK 50253 – 12 hr/50 Hz or 24 hr/50 Hz
- MK 50254 – 12 hr/60 Hz or 24 Hr/60 Hz

24 hr. Alarm
Snooze Alarm



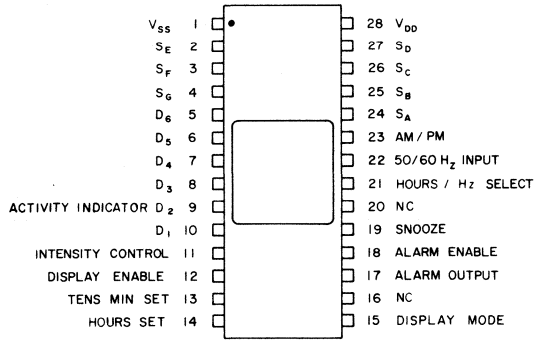
FUNCTIONAL DIAGRAM



DESCRIPTION

The MK 50250 is a versatile MOS/LSI clock circuit manufactured by MOSTEK using its depletion-load, ion implantation process and P-channel technology. The circuit can be used to construct a digital alarm clock with the addition of only a simple power supply, display, and standard interfacing components. (See Typical Circuit Configuration). The circuit is compatible with 4 or 6 digit seven segment multiplexed displays. An AM/PM and circuit activity signal is generated by the chip. The alarm operates in a 24 hour mode, which allows the alarm to be disabled and immediately reenabled to activate 24 hours later. The snooze inhibits an activated alarm for 10 minutes.

PIN CONNECTIONS



CONSUMER CIRCUITS

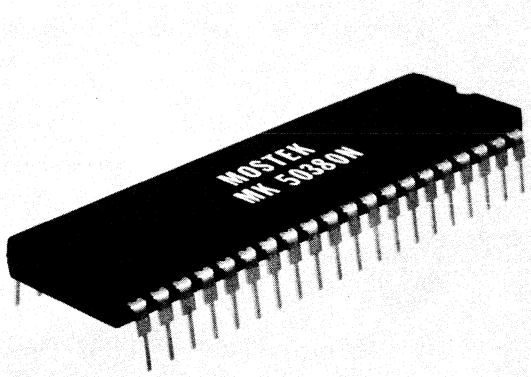
MK50380N
MK50381N

MOS Clock Radio Circuit

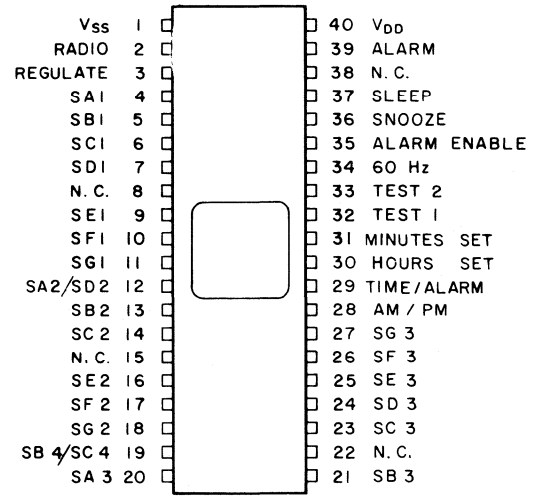
MOSTEK

FEATURES:

- ☐ Direct drive display outputs
- ☐ 10 mA. D.C. per segment
- ☐ Current control regulation — on chip
- ☐ Low power brightness control — on chip
- ☐ RFI eliminating slow-up circuitry
- ☐ SLEEP radio feature
- ☐ 24-hour "SNOOZE" alarm
- ☐ Independent digit setting
- ☐ Multiple ground pins for high reliability
- ☐ Non-multiplexed output circuitry
- ☐ MK 50380N—12 hr/60 Hz
- ☐ MK 50381N—12 hr/50 Hz



PIN CONNECTION



DESCRIPTION

The MK 50380 provides the logic, timing and display interface circuitry for a completely solid state digital clock-radio. The circuit realizes a goal of minimal system cost while maintaining a high standard of performance and reliability.

The MK 50380 features direct drive display outputs eliminating all components (active or passive) between the circuit and LED display. These outputs are capable of sourcing 10 mADC @ 45° C consistently and reliably.

Consistency is provided by on-chip current control regulation. This minimizes inadequate brightness, overheating or other production difficulties.

Reliability is provided by multiple ground pads connected internally (1, 8, 15, 22) and extended (V_{SS}) metal width. This minimizes the danger of long term failures due to metal migration at high current levels.

Each display buffer is driven by slow-up circuitry to eliminate the troublesome RFI present in most multiplexed and some non-multiplexed designs.

The "ALARM" output features 24 hour setting capability "SNOOZE" (6-7 minutes) inhibit, and disable circuitry. This output is a logic "1" level when activated and not inhibited or disabled. A separate "RADIO" output may be enabled for approximately 1 Hr. unless cancelled prematurely by subsequently activating the "SNOOZE" feature.

The "TIME/ALARM" input selects the function to be displayed. The "HOURS SET" input advances the displayed hours when activated. The "MINUTES SET" input advances the displayed minutes digit when activated. Simultaneously activating both the "HOURS SET" and "MINUTES SET" inputs advances the displayed tens of minutes digit. These units are advanced independently at a 1 Hz rate.

The MK 50380 is an MOS/LSI clock-radio circuit manufactured by MOSTEK using its depletion load, ion implantation process and P-Channel technology.

CONSUMER CIRCUITS

PRELIMINARY

MK50440M

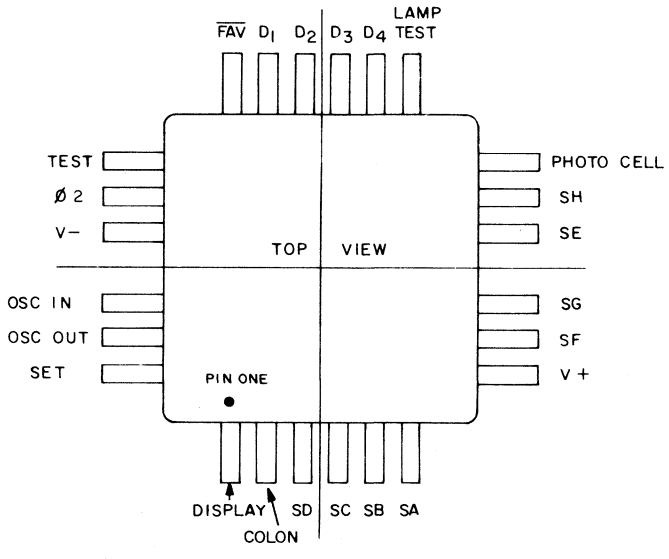
CMOS LED Watch Circuit

MOSTEK

FEATURES:

- ☐ Hours, minutes, seconds, month, day and date.
- ☐ Oscillator inverter for 32,768Hz quartz crystal.
- ☐ Direct segment drive with on-chip-current limiting resisters.
- ☐ Single pole "close to case" switch input with internal debounce for display and time setting.
- ☐ 1024 Hz output for oscillator trimming.
- ☐ Intensity control.

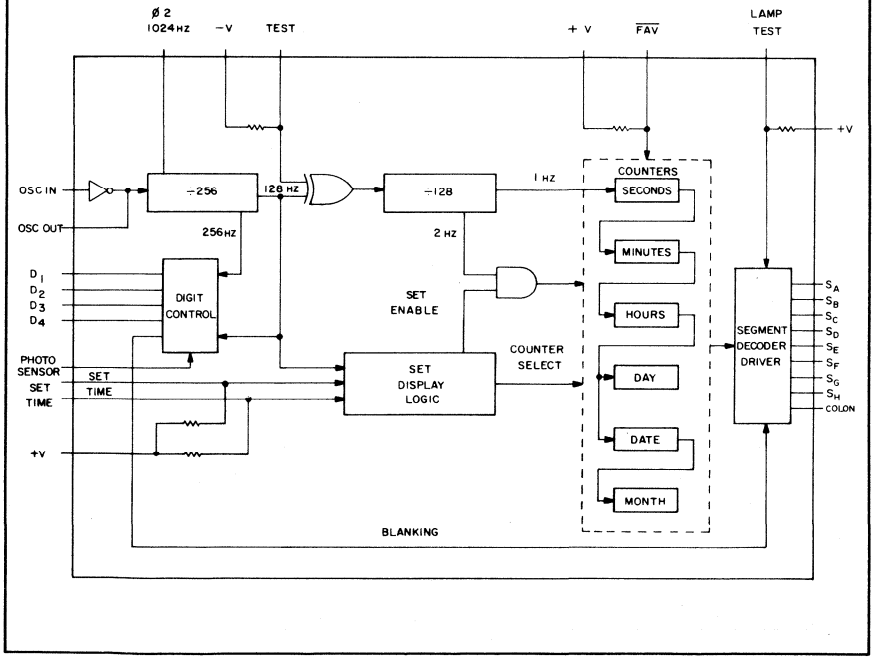
PIN CONNECTIONS



DESCRIPTION:

The MK 50440, is a single chip ion-implanted metal gate CMOS circuit for multiplexed four digit LED display calendar watches. The circuit provides 12 hour time-keeping with a 4-year month-date calendar, and displays day of the week. The MK 50440 displays month-left and date right. A single "close-to-case" switch is used for display and features display time-out. An additional switch input is used for time setting.

FUNCTIONAL DIAGRAM



CONSUMER CIRCUITS

MEMORIES
MICRO-PROCESSORS
CONSUMER CIRCUITS
INDUSTRIAL

FUTURE PRODUCTS

MOSTEK

TO BE ANNOUNCED

MK29000P

16K-BIT
MOS Read Only Memory

MOSTEK

FEATURES:

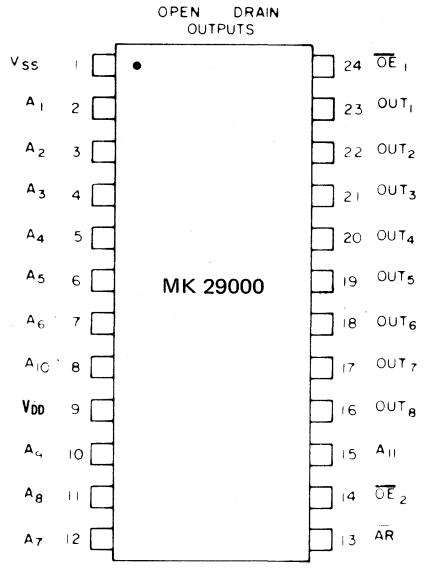
* Fast Access, Less Than 250 ns Access Time
* Single +12 Volt Power Supply
* Low Power Dissipation
* 2K x 8 or 4K x 4 Organization With Open-Drain Outputs
* Ion-Implanted for TTL/DTL Compatibility at All Inputs
* Input Protection Against Static Charge
* On-Chip Address Latches

DESCRIPTION:

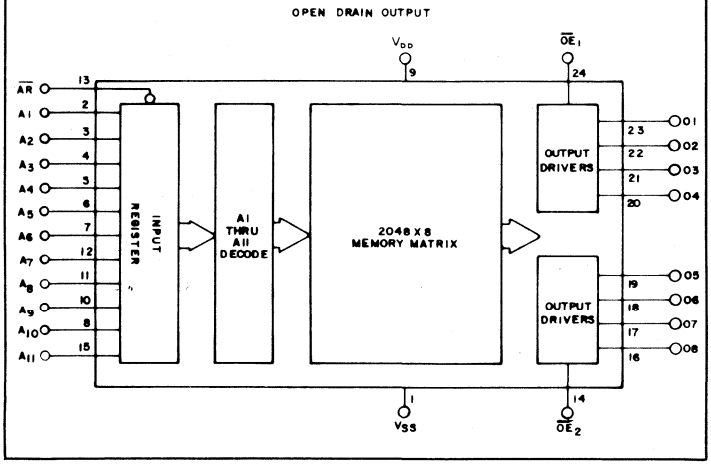
The MK 29000 is a mask programmable dynamic, read only memory circuit fabricated with MOSTEK's special Self-Aligned, N-Channel, Metal Gate process to minimize chip size and optimize circuit performance. The MK 29000 is the first of a series of high performance ROM circuits designed to be competitive with many bipolar ROMs in speed, but excel in power dissipation and bit density. The timing requirements for the MK 29000 are such that the part will fit right into many high performance memory systems. The $\overline{RAS}$ and precharge timing requirements for the MK 4096, 4K dynamic RAM, are identical to the $\overline{AR}$ and precharge requirements of the MK 29000.

The MK 29001 is a preprogrammed version of the MK 29000 containing six character conversion codes (ASCII to Selectric, EBCDIC, and a modified 8-bit Hollerith/Selectric to ASCII, EBCDIC to ASCII, and a modified Hollerith to ASCII) as well as 128 USASCII characters using mixed character fonts of 5 x 7 and 7 x 7 dot matrices with extra check bits.

PIN CONFIGURATION



BLOCK DIAGRAM



FUTURE PRODUCTS

TO BE ANNOUNCED

MK31000P

16K-BIT

MOS Read Only Memory

MOSTEK

FEATURES:

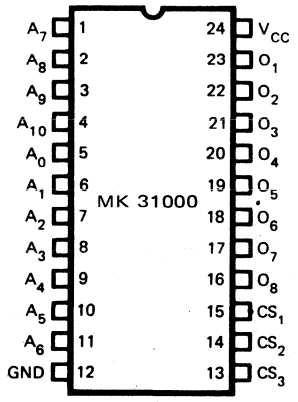
- ☐ Single +5 volt power supply
- ☐ Completely static operation (no clocks required)
- ☐ Less than 600 ns Access Time
- ☐ Directly TTL compatible
- ☐ Three programmable chip select inputs
- ☐ Input protection against static charge

DESCRIPTION:

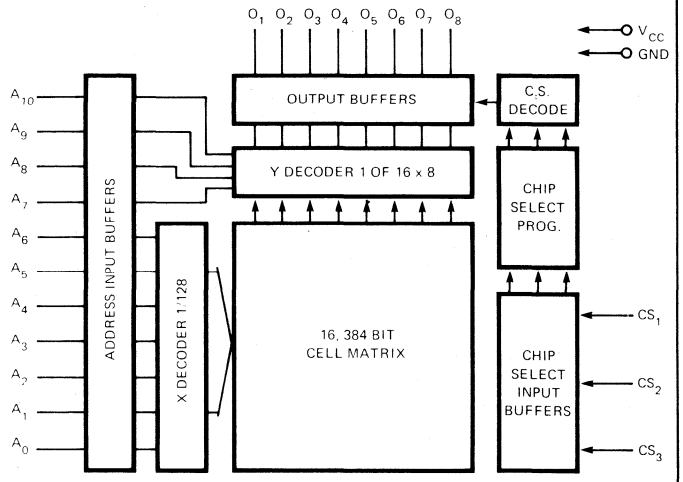
The MK 31000 is a 16,384 bit read only memory circuit designed as a high performance replacement for the INTEL 2316. The internal organization of the MK 31000 is arranged as a 2K x 8 matrix to allow simple interface with eight-bit processor applications. The static operation of the MK 31000 coupled with three programmable chip select inputs provide an easily expandable, high performance memory circuit with extremely simple interface requirements.

The MK 31000 read only memory is fabricated with N-Channel silicon gate technology to minimize chip size and optimize circuit performance. Ion implantation allows TTL compatibility at both the inputs and the outputs.

PIN CONFIGURATION



FUNCTIONAL DIAGRAM



FUTURE PRODUCTS

TO BE ANNOUNCED

MK4027P

4096x 1 **BIT DYNAMIC**

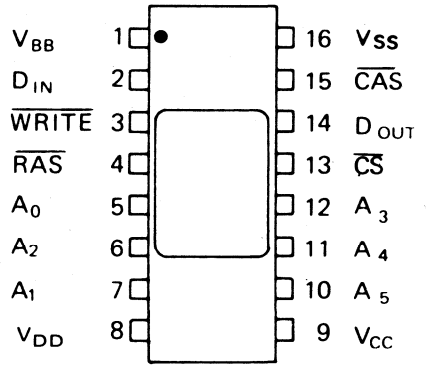
Random Access Memory

MOSTEK

FEATURES:

* Standard 16-pin DIP
* All Inputs are Low Capacitance and TTL Compatible
* Input Latches for Addresses, Chip Select and Data In
* Inputs Protected Against Static Charge
* Three-State TTL Compatible Output
* Output Data Latched and Valid Into Next Cycle
* Pin Compatible with MK 4096
* Improved Performance With Page-Mode and Read-Modify-Write Capability:
  Random read or write cycles under 325 ns
  Random access under 200 ns
  Page access under 125 ns
* Low Power: Active power under 500 mW
  Standby power under 12mW
* No Power-up Sequence Requirement

PIN CONFIGURATION



DESCRIPTION:

The MK 4027 is a 4096X1 bit dynamic random access memory circuit fabricated with Mostek's N-Channel silicon gate, Isoplanar process. This process allows the MK 4027 to be a high performance state-of-the-art memory circuit that is manufacturable in high volume. The single transistor cell employed in the memory matrix utilizes a dynamic storage technique and each of the 64 row addresses requires refreshing every 2 milliseconds.

A unique multiplexing and latching technique for the address inputs permits the MK 4027 to be packaged in a standard 16-pin DIP on 0.3 inch centers. This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

System oriented features designed into the MK 4027 include direct interfacing capability with TTL, 6 instead of 12 low capacitance address lines to drive, on-chip registers which eliminate the need for interface registers, input logic levels selected to optimize the noise immunity, and two chip-select methods to allow the user to determine the appropriate speed/power characteristics of his memory system. The MK 4027 also incorporates several different and flexible timing modes. Besides the usual read and write cycles, read-modify-write and page-mode timing is possible with the MK 4027. Page-mode timing is very useful in systems that require Direct Memory Access (DMA) operation.

ADDRESSING:

The 12 address bits required to decode 1 of the 4096 cell locations within the MK 4027 are multiplexed onto the 6 address inputs and latched into the on-chip row and column address latches. The Row Address Strobe ($\overline{RAS}$) latches the 6 row address bits into the chip. The Column Address Strobe ($\overline{CAS}$) subsequently latches the 6 column address bits plus Chip Select ($\overline{CS}$) into the chip. The hold time requirement for the column address bits and $\overline{CS}$ is referenced to both $\overline{RAS}$ and $\overline{CAS}$. Since the Chip Select signal is not required until well into the memory cycle, its decoding time does not add to system access or cycle time.

FUTURE PRODUCTS

TO BE ANNOUNCED

MK 50396N
MK 50397N

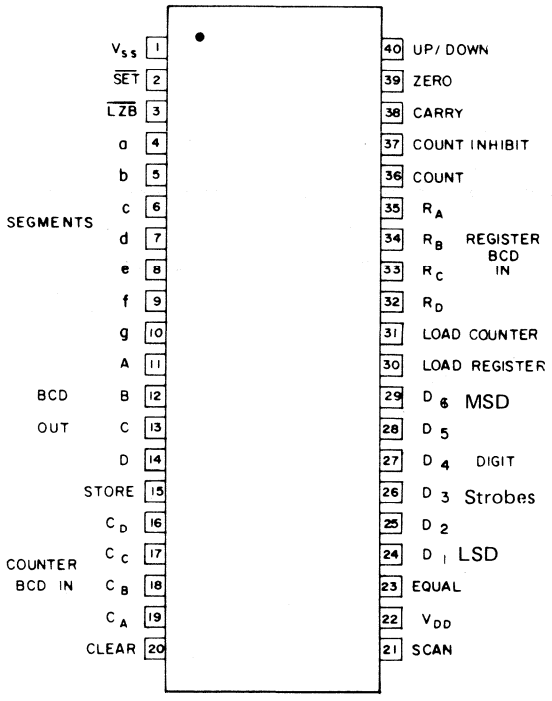
MOS Six-Decade Counter/Display Decoder

MOSTEK

FEATURES:

- ☐ Single power supply
- ☐ Schmitt-Trigger on the count-input
- ☐ Six decades of synchronous up/down counting
- ☐ Look-ahead carry or borrow
- ☐ Loadable counter
- ☐ Loadable compare-register with comparator output
- ☐ Multiplexed BCD and seven-segment outputs
- ☐ Internal scan oscillator
- ☐ Direct LED segment drive
- ☐ Interfaces directly with CMOS logic
- ☐ Leading zero blanking
- ☐ MK 50396 programmed to count time: 99 hrs., 59 min., 59 sec.
- ☐ MK 50397 programmed to count time: 59 min., 59 sec., 99/100 sec.

PIN CONNECTION



DESCRIPTION:

The MK 50395 Series is an ion-implanted, P-channel MOS six-decade synchronous up/down-counter/display driver with compare-register and storage-latches. The counter as well as the register can be loaded digit-by-digit with BCD data. The counterhas an asynchronous-clear function.

Scanning is controlled by the scan oscillator input which is self-oscillating or can be overdriven by an external signal. The six-decade-register is constantly compared to the state of the six-decade-counter and when both the register and the counter have the same content, an EQUAL signal is generated. The contents of the counter can be transferred into the 6-digit latch which is then multiplexed from MSD to LSD in BCD and 7-segment format to the output. The seven-segment decoder incorporates a leading-zero blanking circuit which can be disabled by an external signal. This device is intended to interface directly with the standard CMOS logic families.

TO BE ANNOUNCED

MK5085N
MK5086N

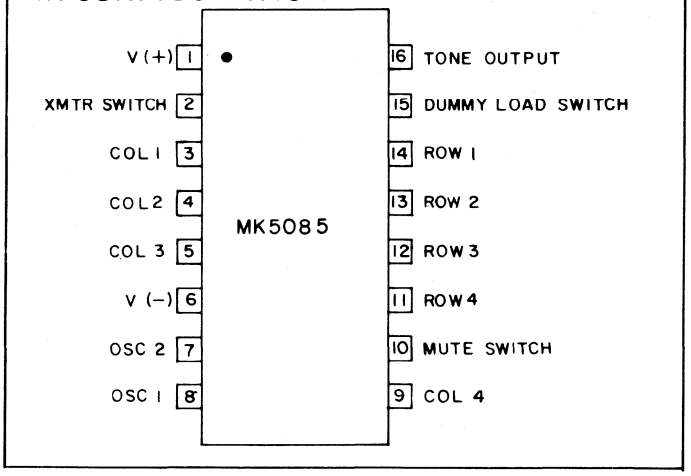
Integrated Tone Dialer

MOSTEK

FEATURES

- Can operate directly from the telephone line with no external power supply
- High accuracy tones
- Long term stability
- Digital divider logic, resistive ladder network, and CMOS operational amplifier on single chip
- Uses inexpensive 3.58 MHz crystal
- Wide supply tolerance suitable for DC supply such as 4AA cells or a single 9 volt battery

PIN CONFIGURATION



DESCRIPTION:

The MK 5085 and MK 5086 are monolithic integrated circuits fabricated with the complementary symmetry MOS (CMOS) process. Using an inexpensive crystal reference, the MK 5085 and MK 5086 provide eight different audio sinusoidal frequencies, which are mixed together to provide tones suitable for Dual-Tone Multi-Frequency telephone dialing.

The keyboard entries select the proper digital dividers to divide the 3.58 MHz to obtain the unique audio frequencies required. These digital signals are then processed by a conventional R-2R ladder network, and current to voltage transformation is made by an on chip amplifier. This is a conventional D to A converter, and yields sine waves of sufficient purity as to require little or no filtering. The same amplifier accomplishes summing of the low and high group tones to obtain the required dual tone signal. Inherent frequency accuracy is obtained via the crystal reference without need for adjustment.

The primary use of the 5085 and 5086 is intended to be used in telephone applications, where it will derive its necessary power directly from the telephone lines, and send the output tones back differentially across these lines. The 5085 and 5086 may also be used with a fixed d.c. supply, and in this case, the audio output tones are available single ended from the output amplifier. The CMOS processing allows operation over a wide range of operating voltages, which implies proper operation over a wide range of loop resistance or a separate supply.

Row and column information may be delivered to the MK 5085 via class A keyboard. The MK 5086 interfaces with the Standard 2 of 7 DTMF Keyboard. Common key functions such as switching out the transmitter and switching in muting resistance are accomplished electronically.

FUTURE PRODUCTS

MOSTEK

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